

FIG. 3

FIG. 3 is a block diagram of a hardware architecture. The diagram shows a central dashed box containing several components: a CONFIG REG (137), a HASH INDEX GEN (131), a MEMORY (133), and COMPARE LOGIC (135). The CONFIG REG (137) is connected to the HASH INDEX GEN (131) and the COMPARE LOGIC (135). The HASH INDEX GEN (131) is connected to the MEMORY (133) and a DBUS (140). The MEMORY (133) is connected to the COMPARE LOGIC (135). The COMPARE LOGIC (135) is connected to the DBUS (140) and an output MF (134). The DBUS (140) is connected to the HASH INDEX GEN (131) and the COMPARE LOGIC (135). The CONFIG REG (137) is also connected to an output MA (136). The MA (136) is connected to an ASSOC STORAGE (111). The ASSOC STORAGE (111) is connected to the DBUS (140). The DBUS (140) is connected to the HASH INDEX GEN (131) and the COMPARE LOGIC (135). The DBUS (140) is also connected to a control bus with signals V, KEY, MSK, PRI, and CNTRL/CFG.

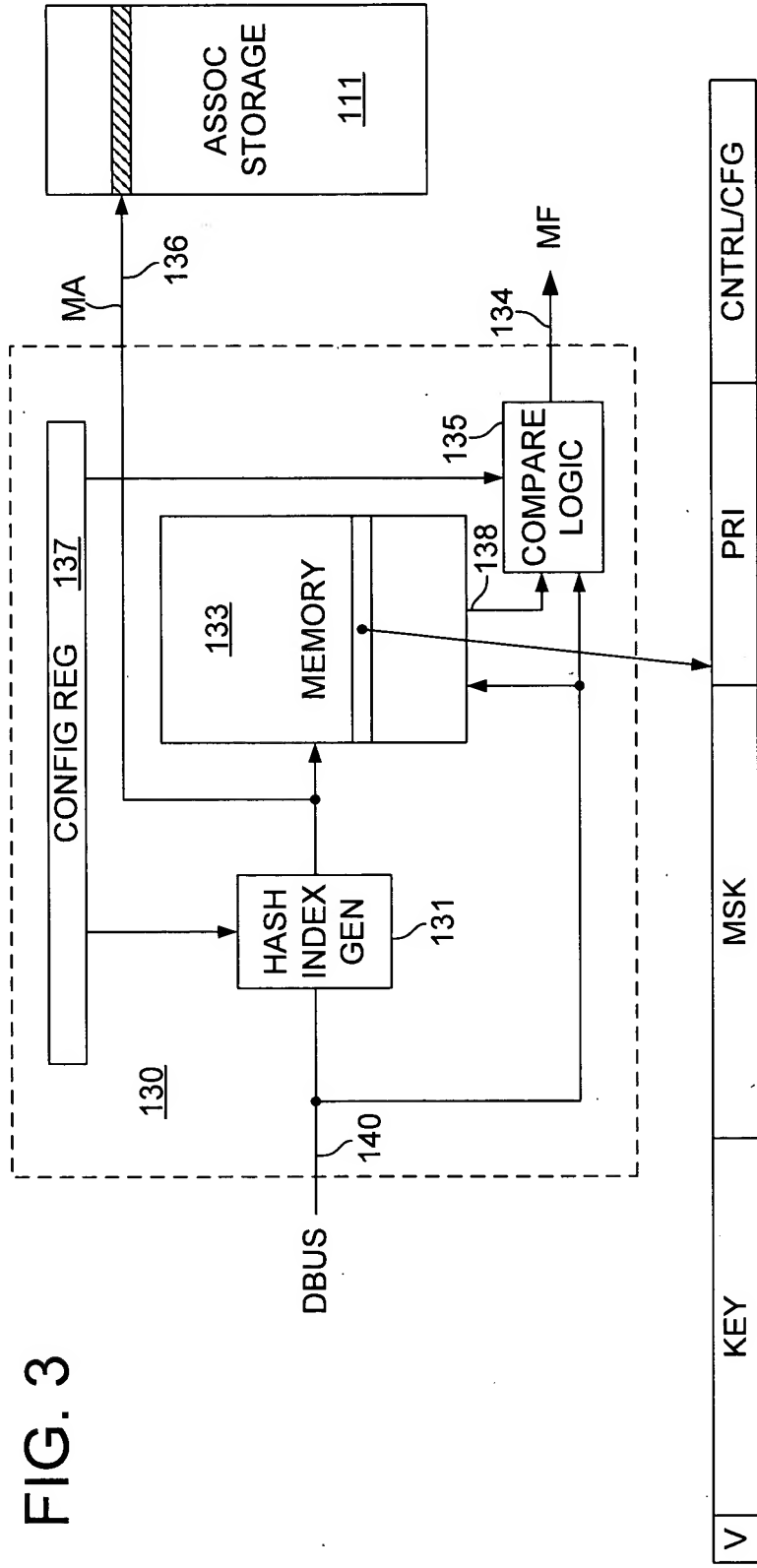


FIG. 4

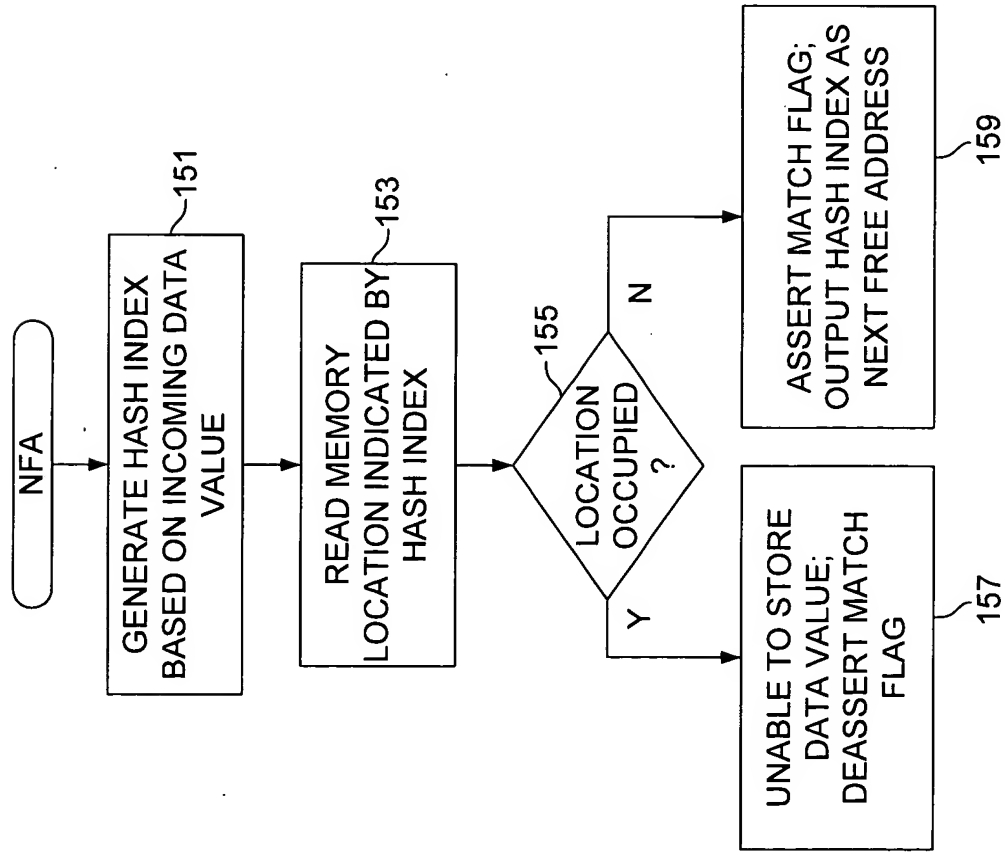
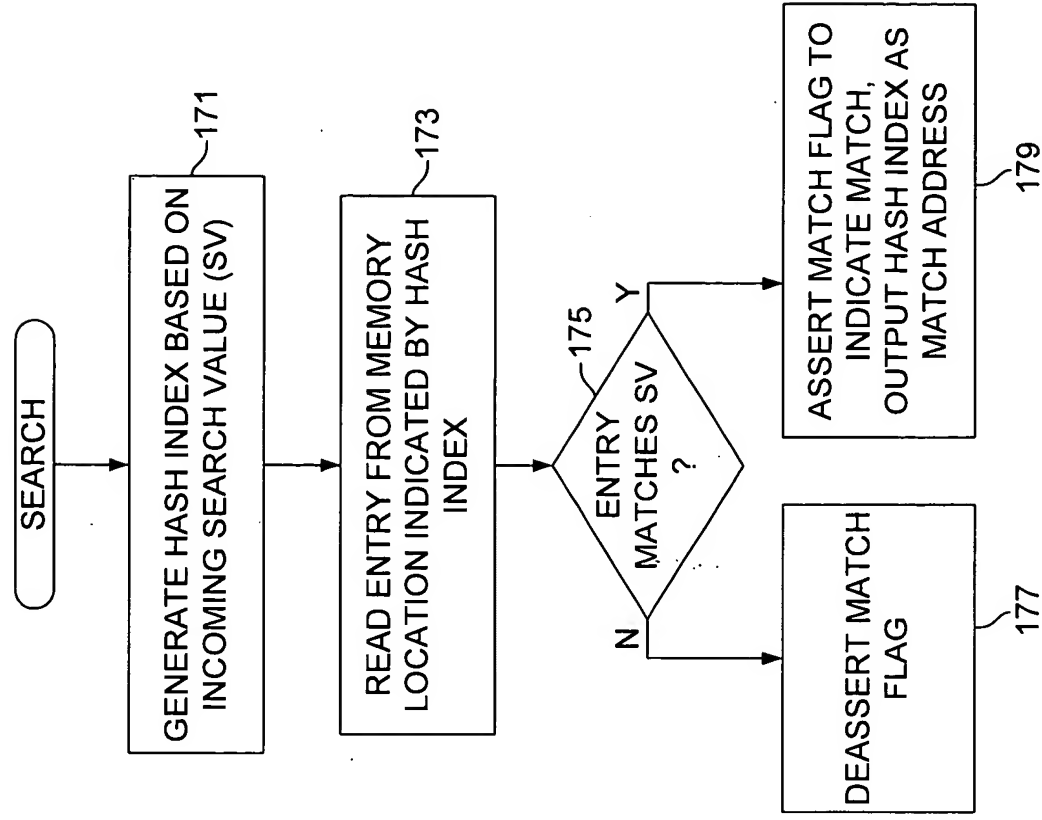


FIG. 5



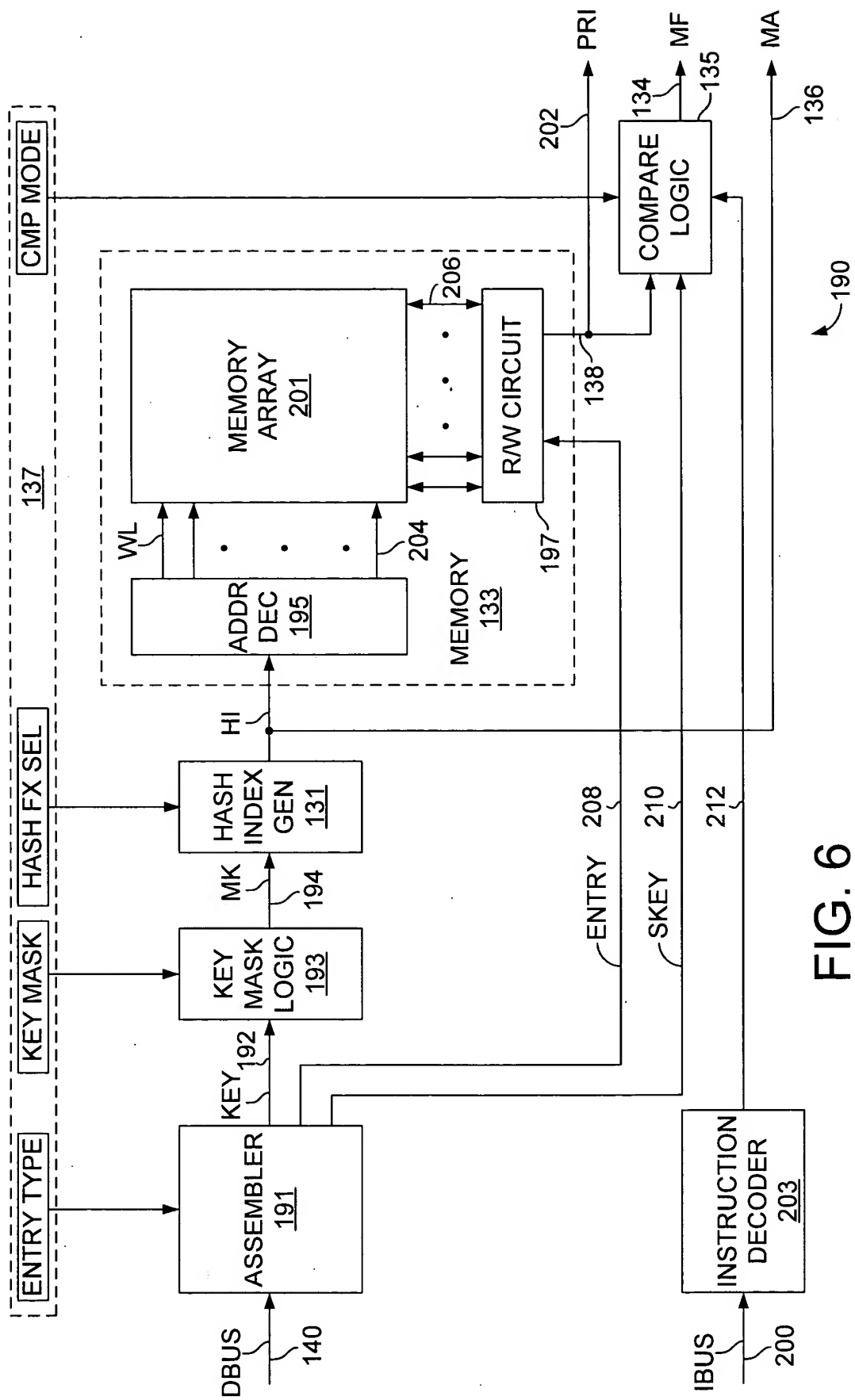


FIG. 6

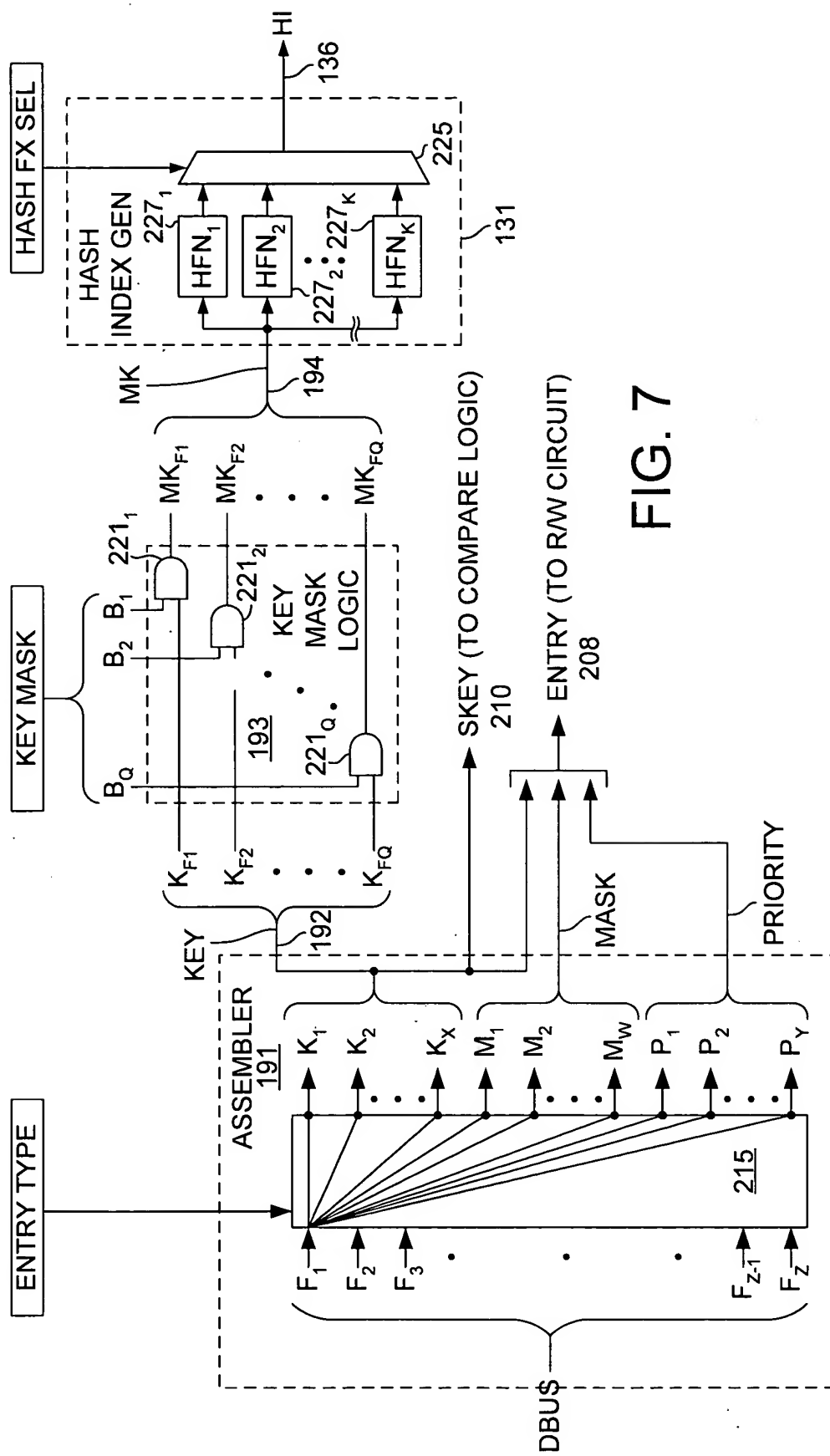
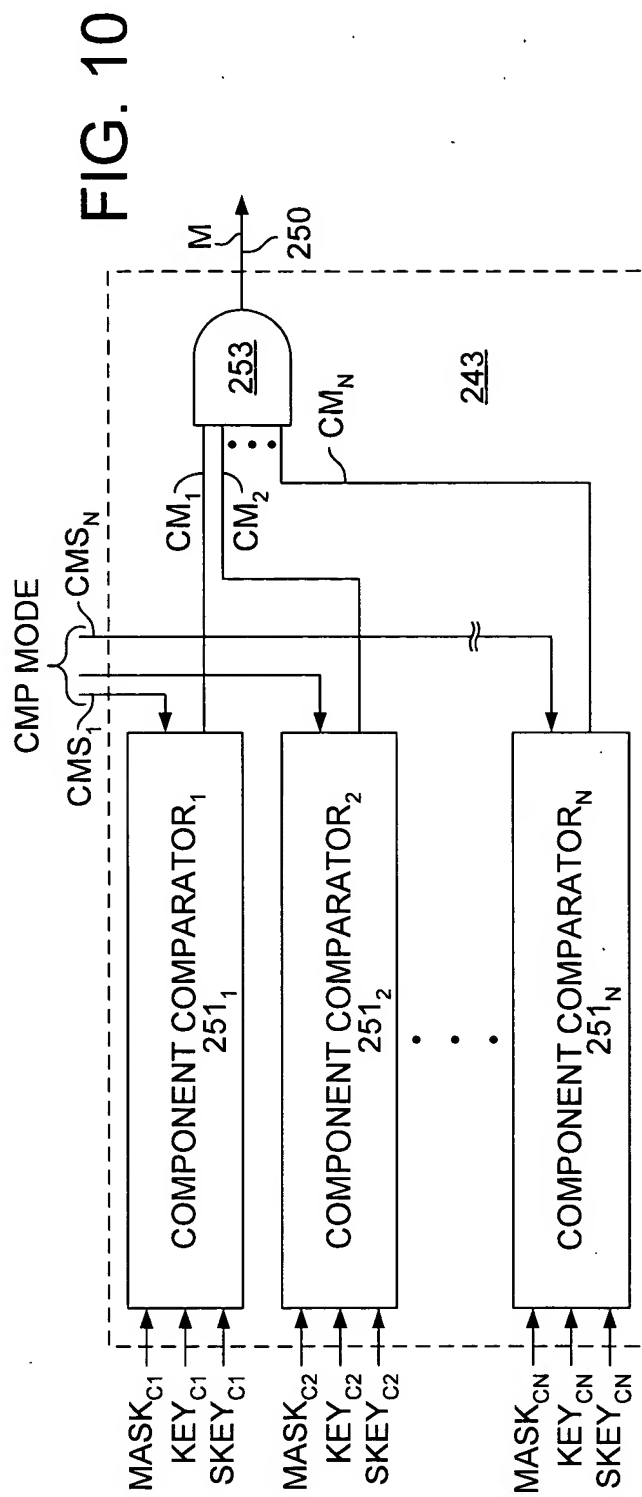
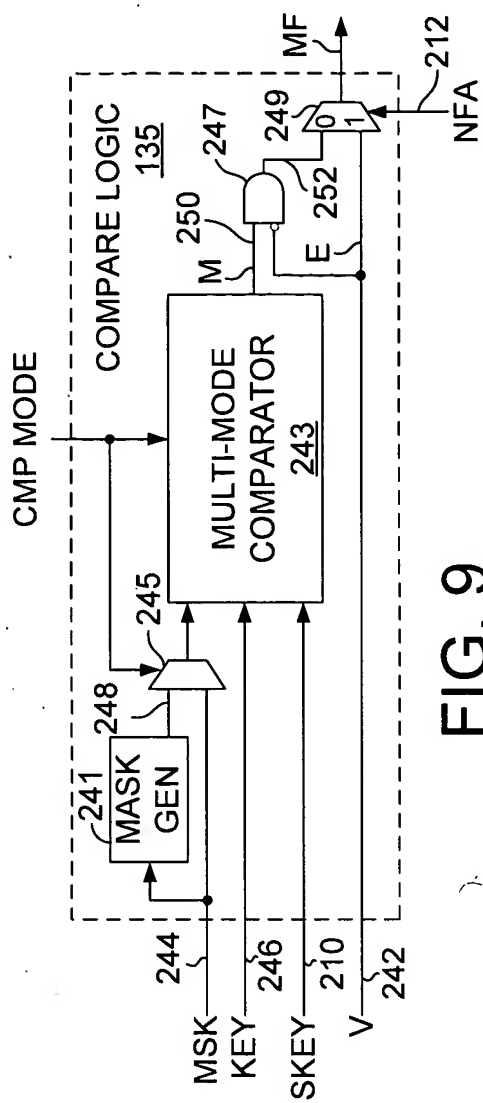
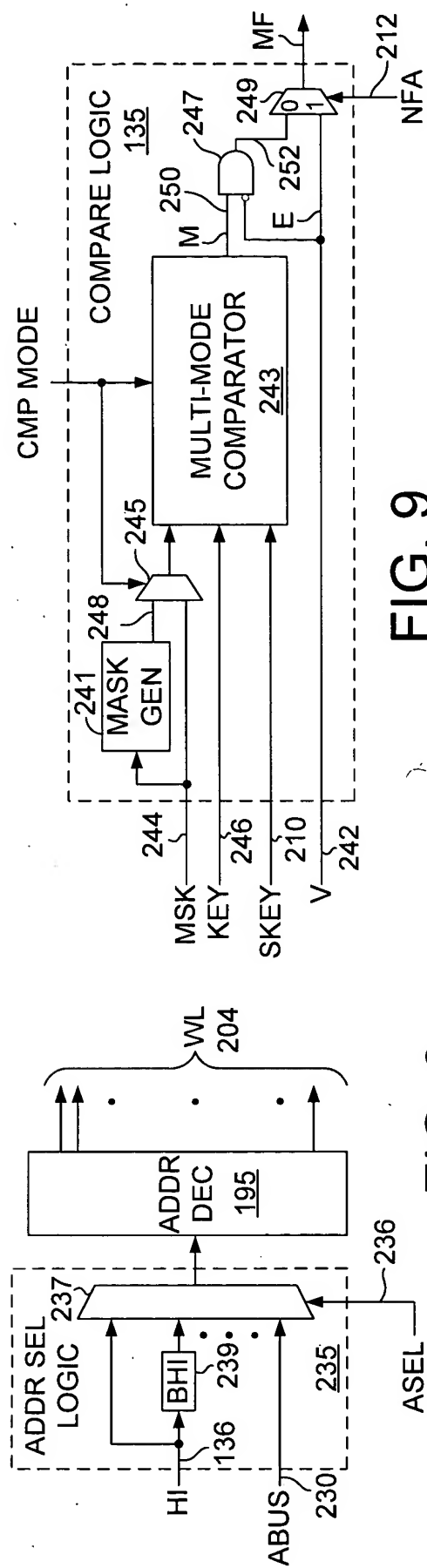


FIG. 7



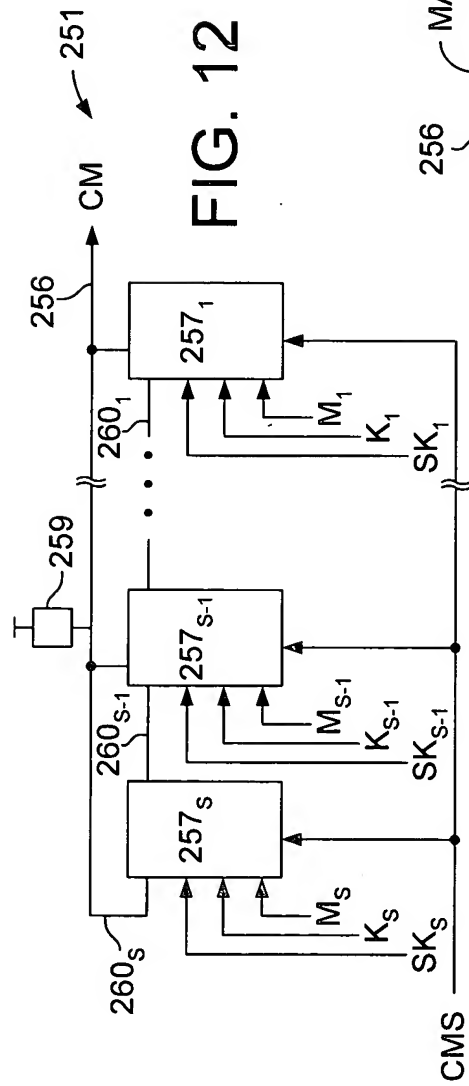


FIG. 12

FIG. 13

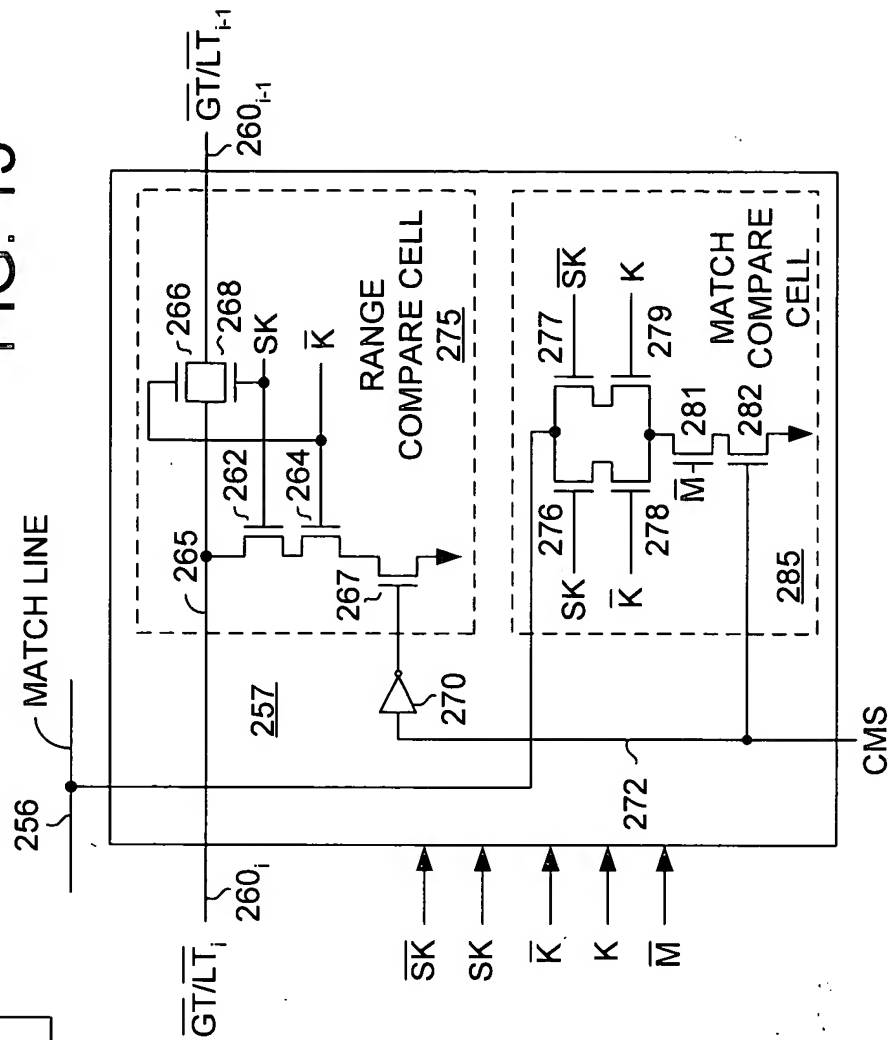
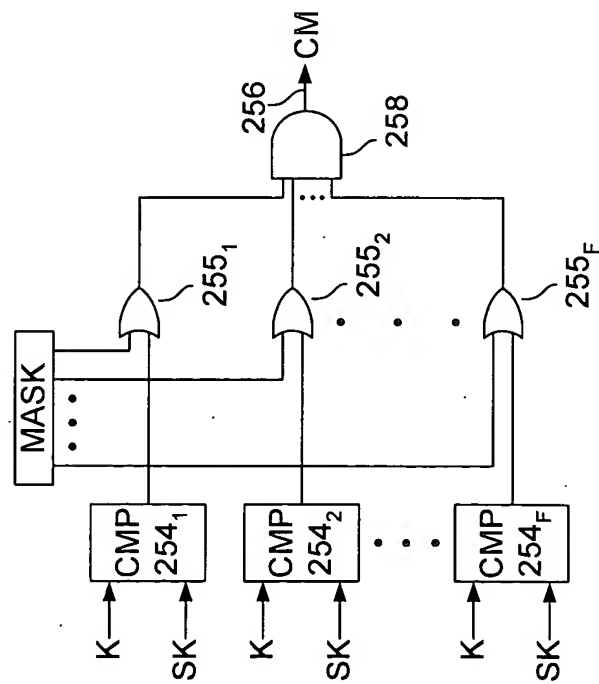


FIG. 11



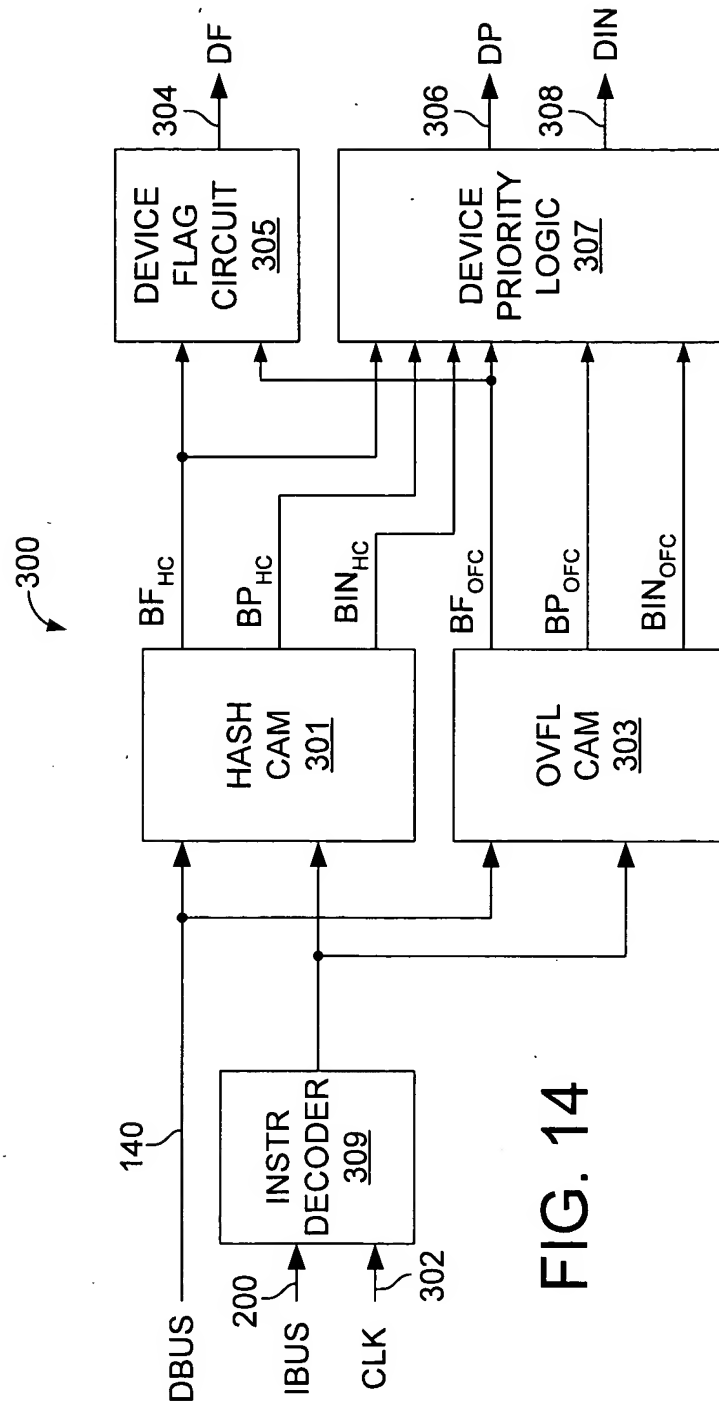


FIG. 14

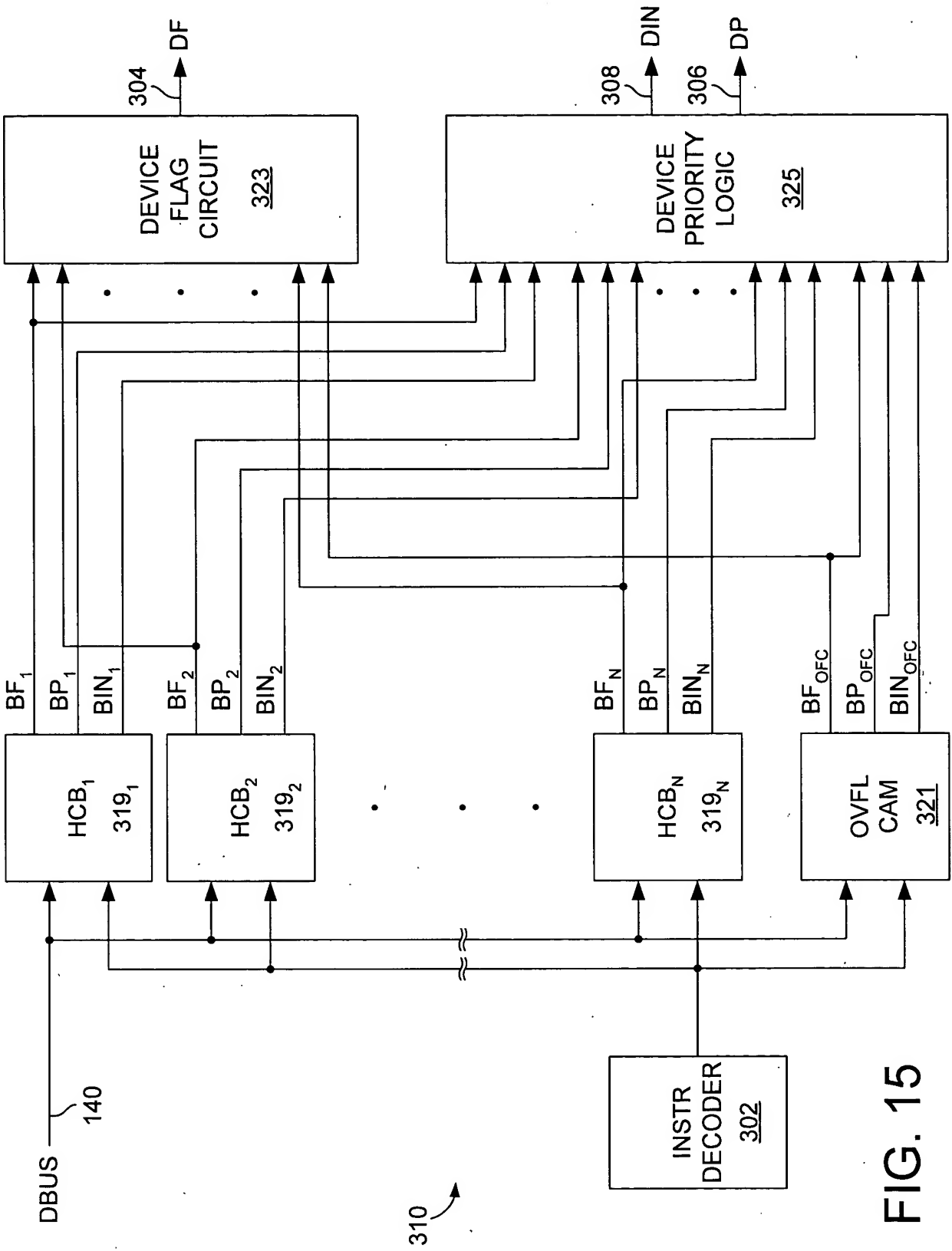


FIG. 15

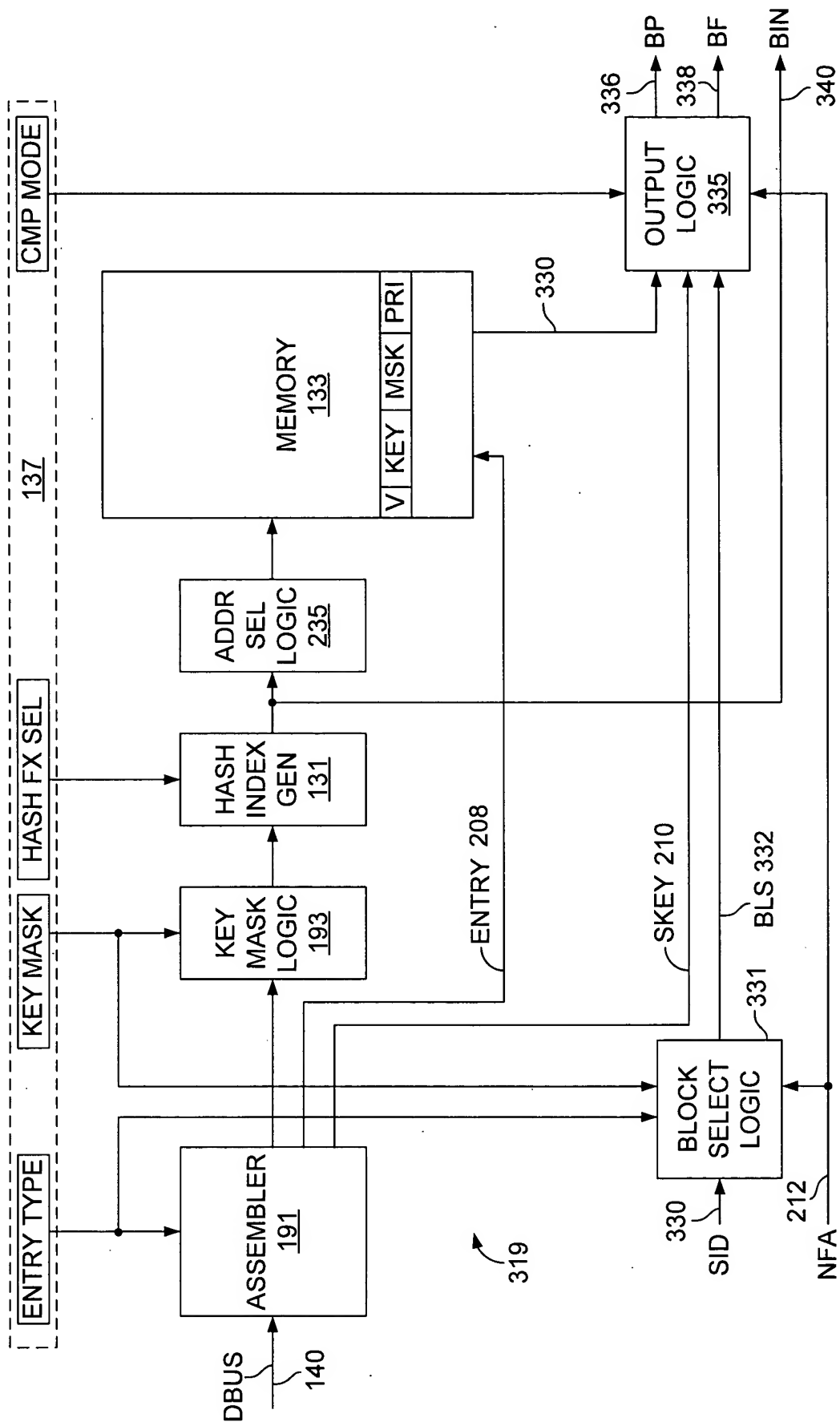
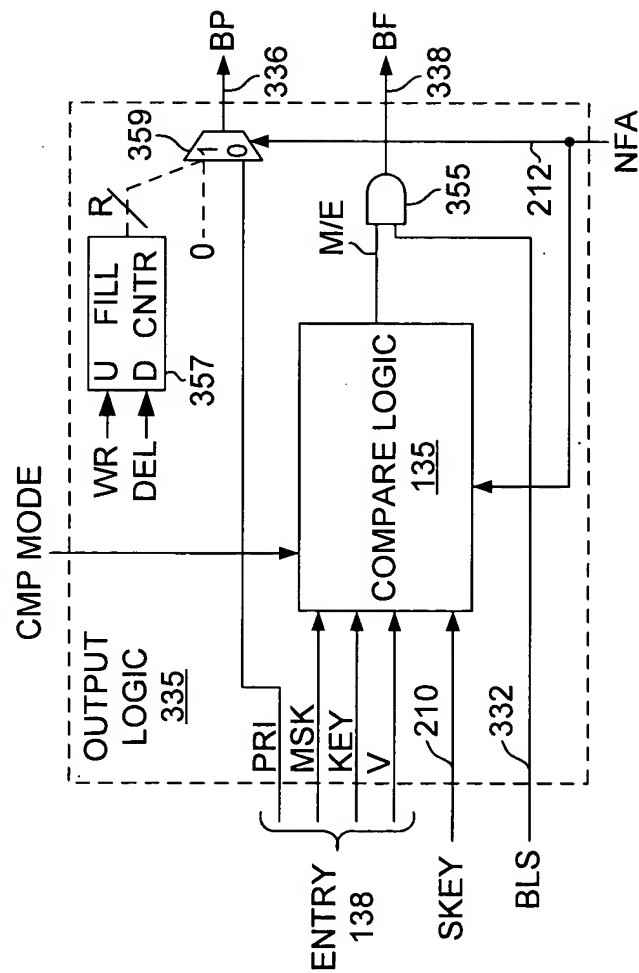
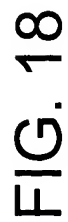
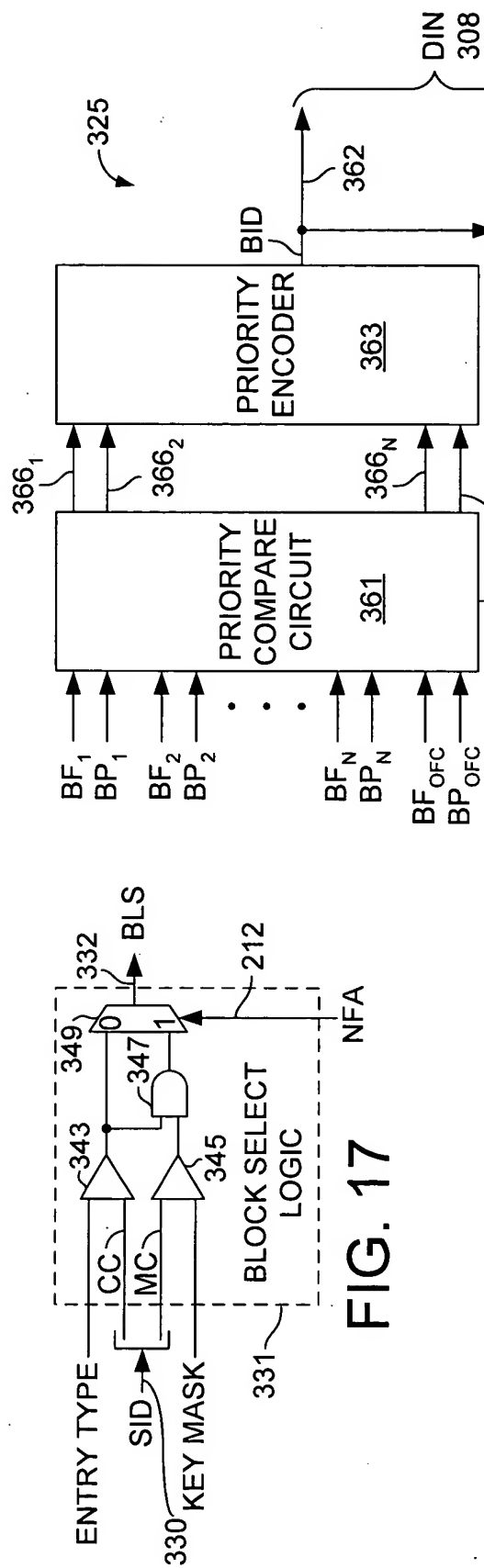
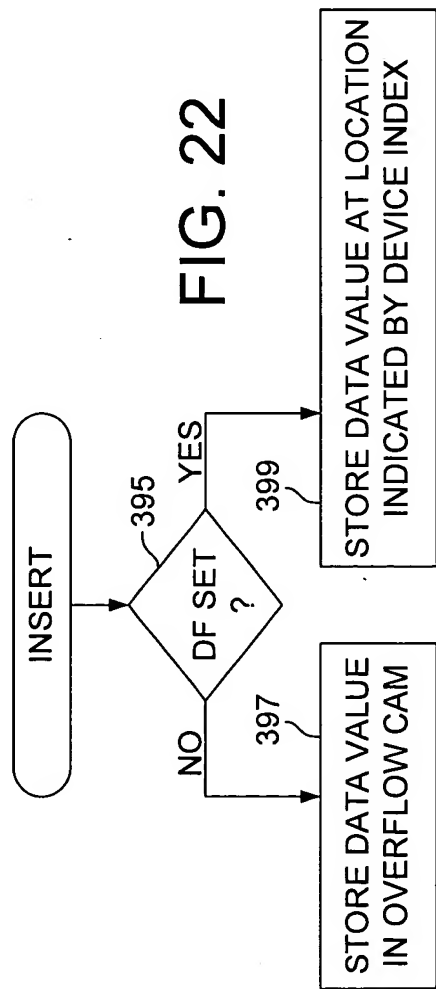
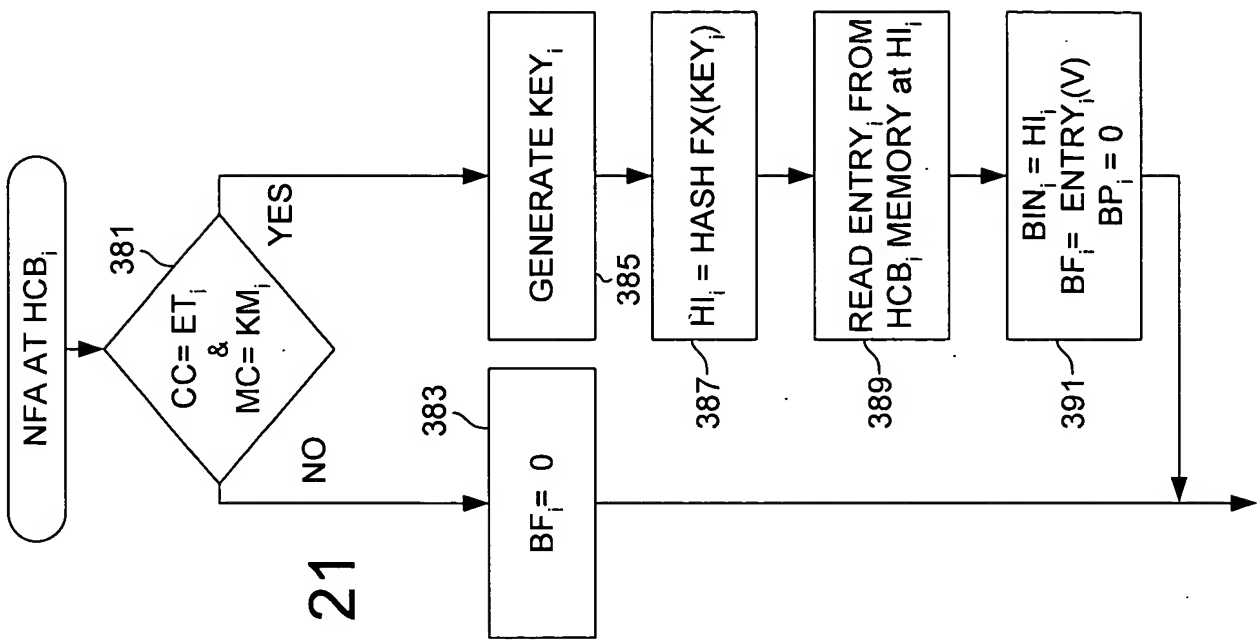
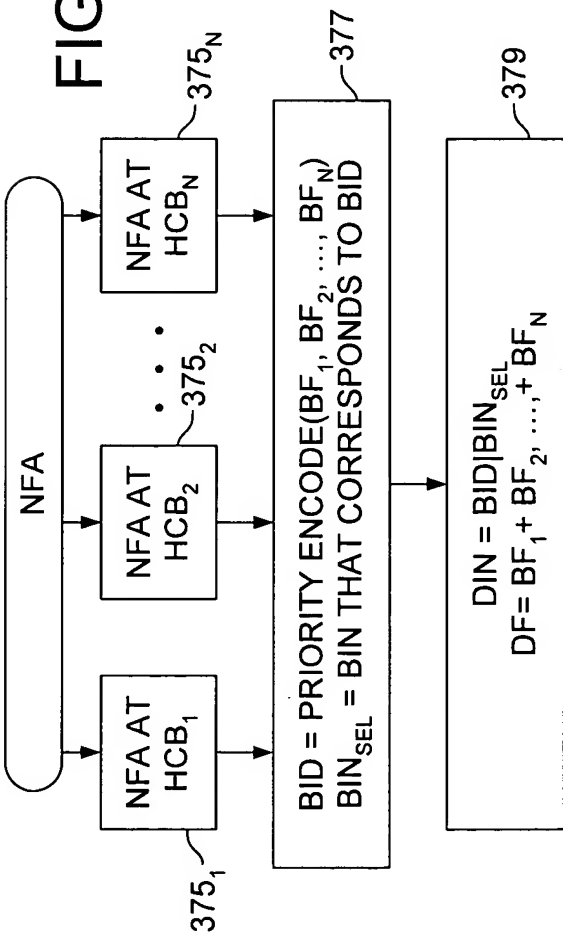


FIG. 16





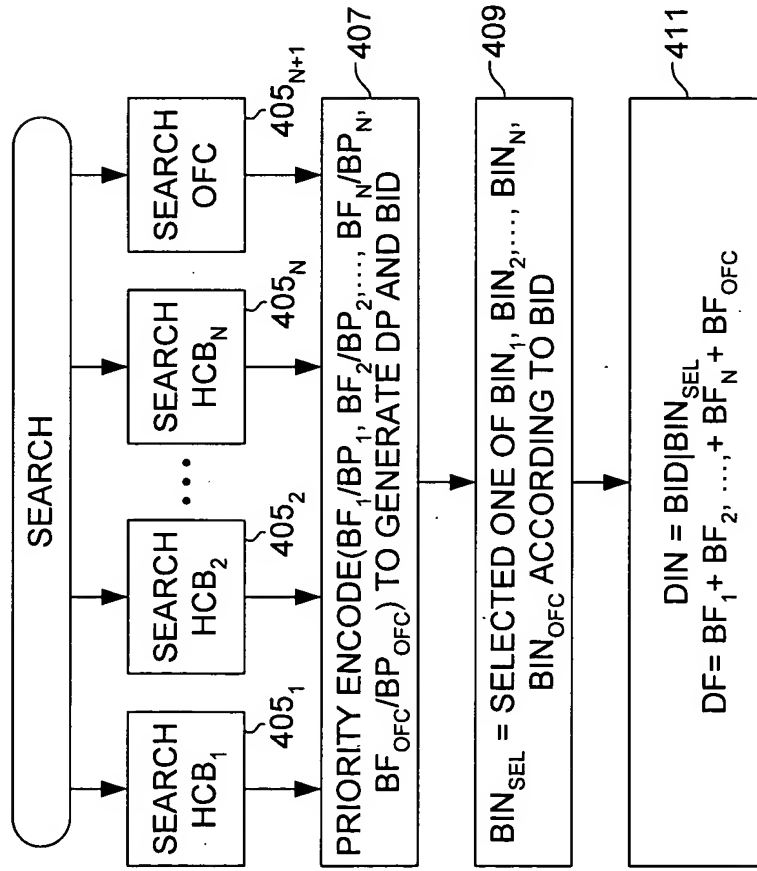


FIG. 23

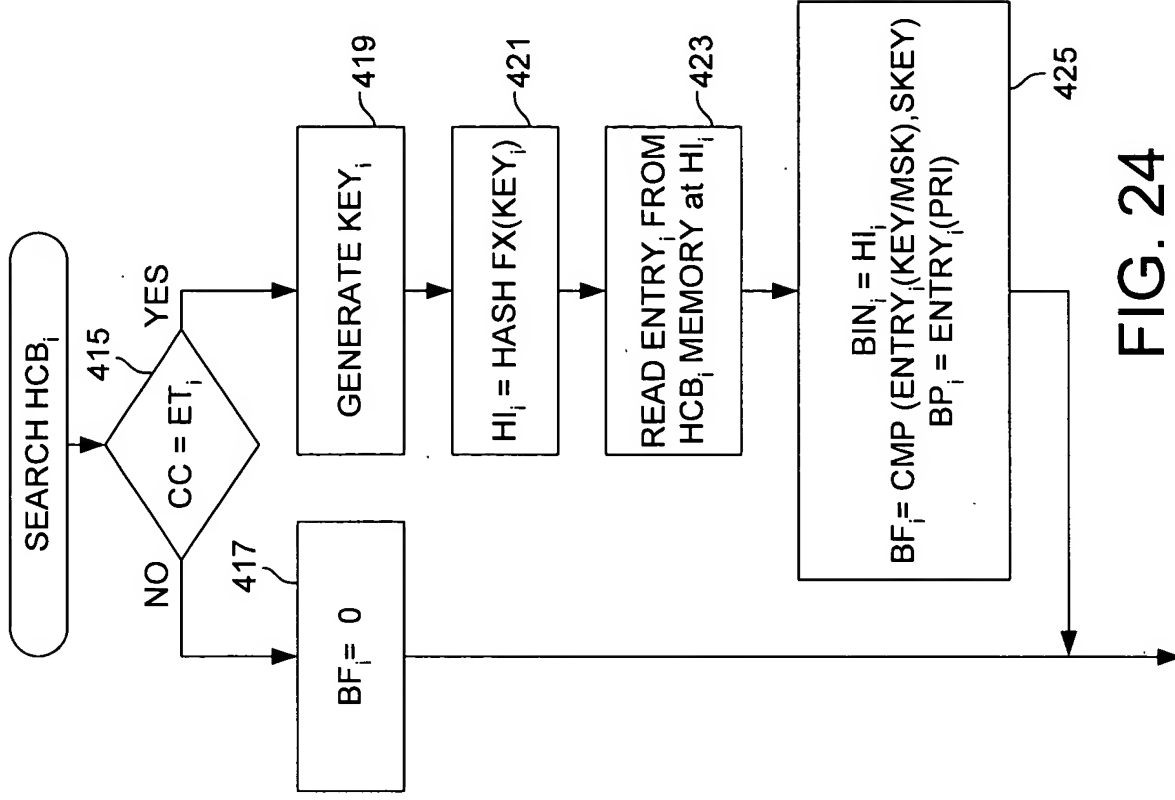


FIG. 24

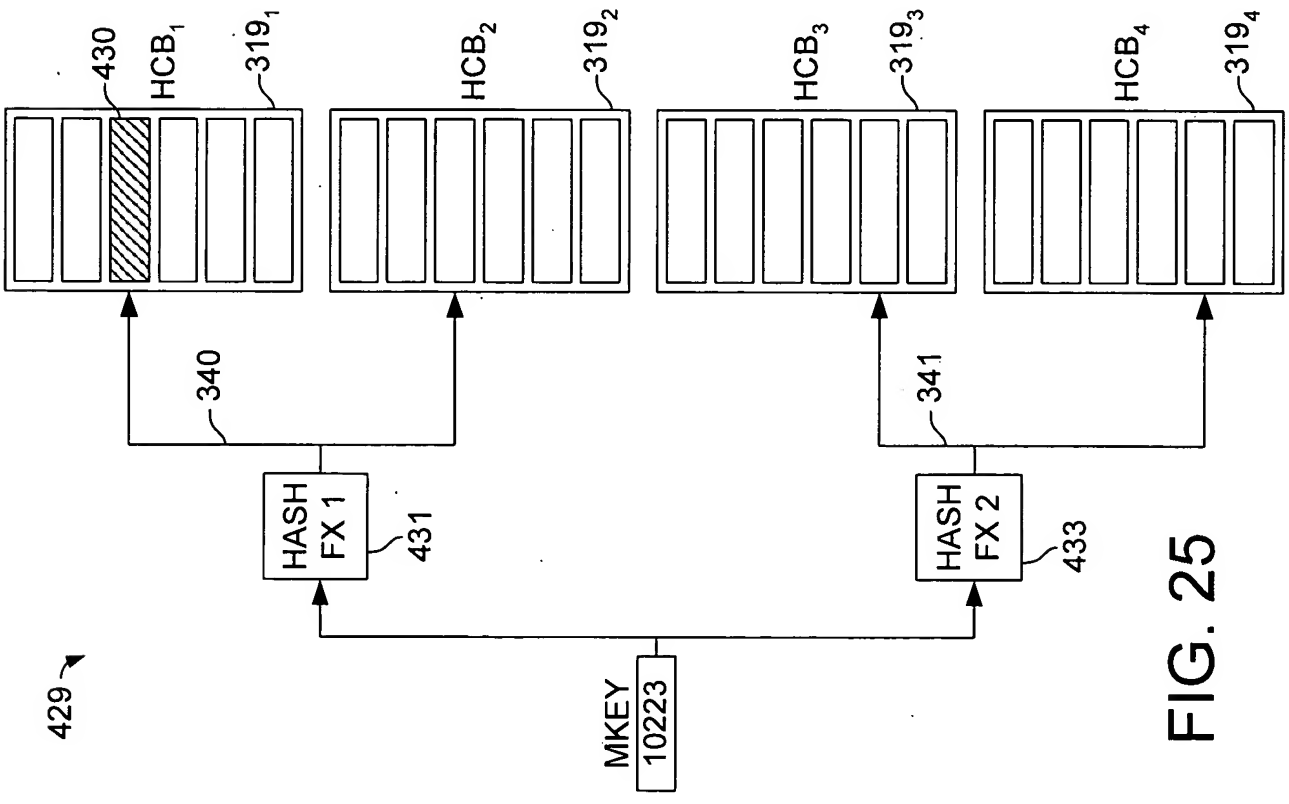


FIG. 25

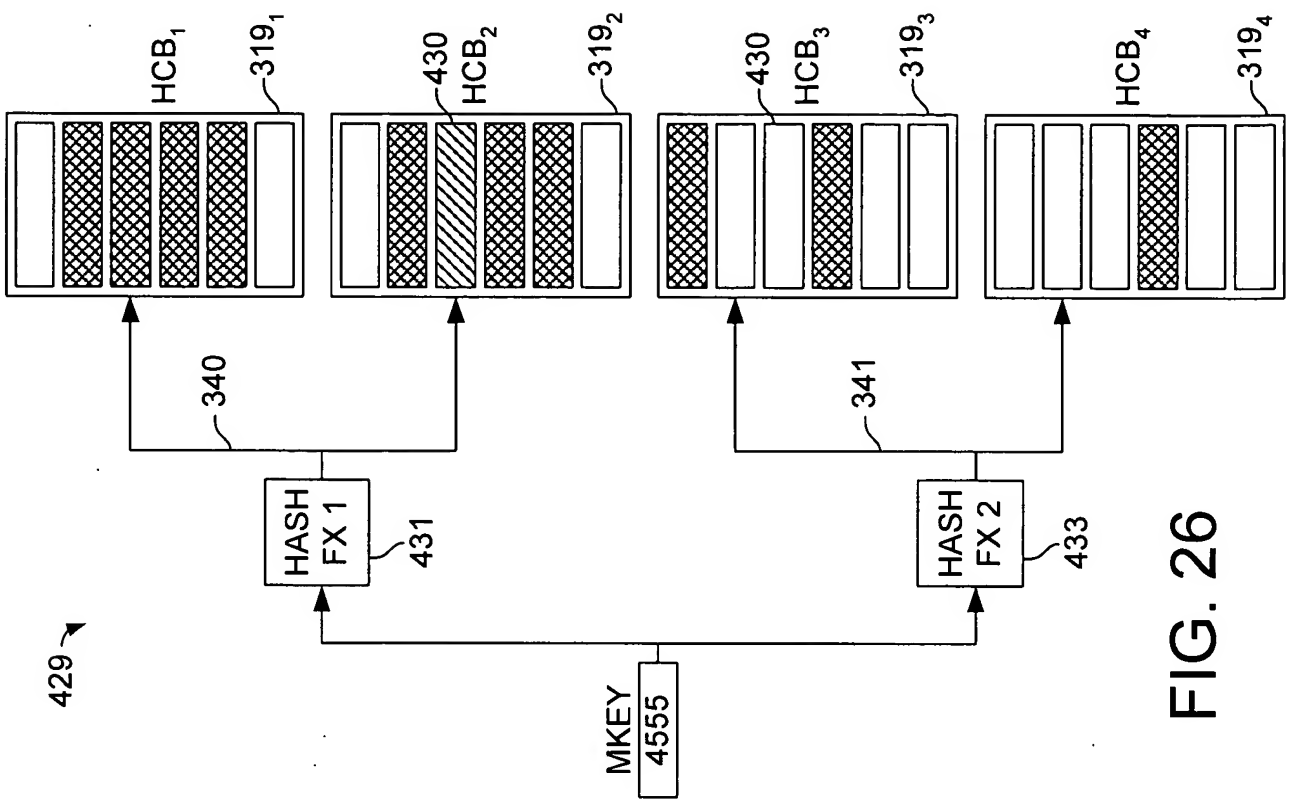


FIG. 26

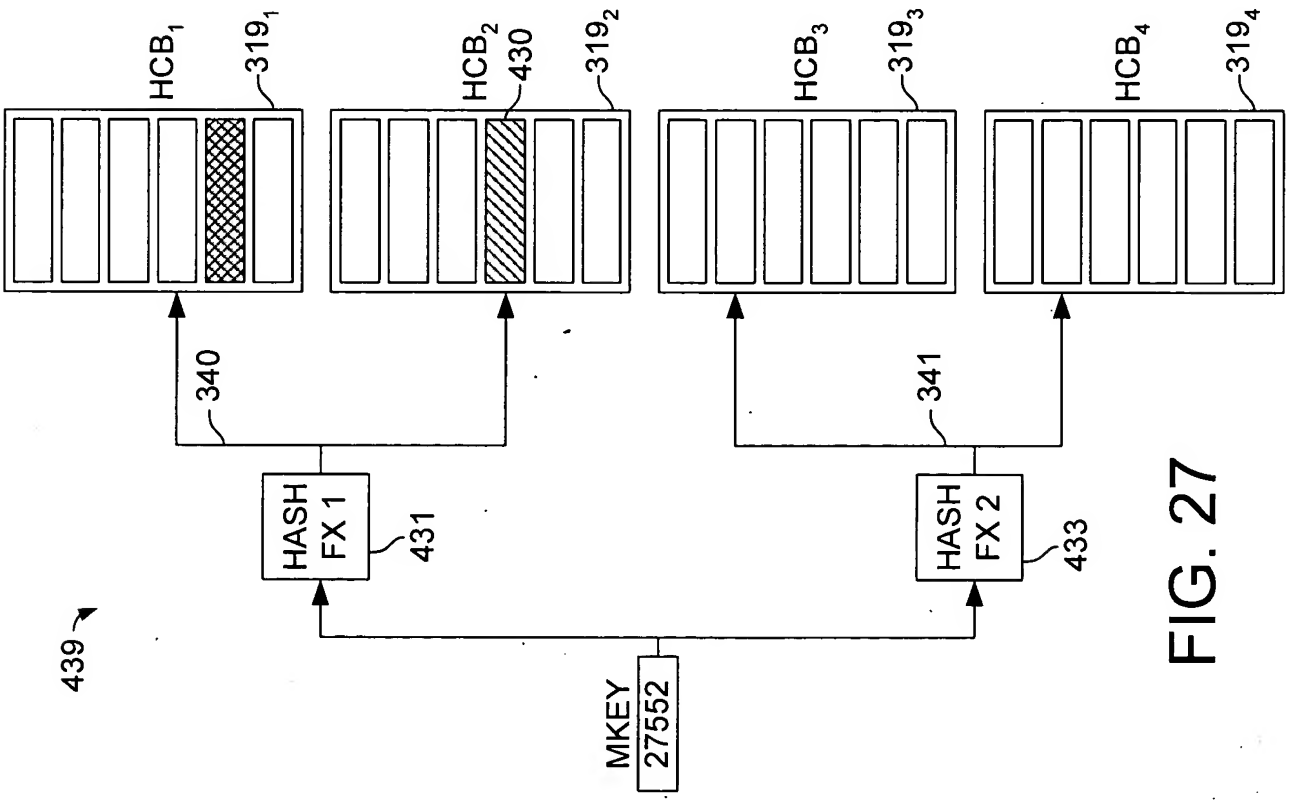


FIG. 27

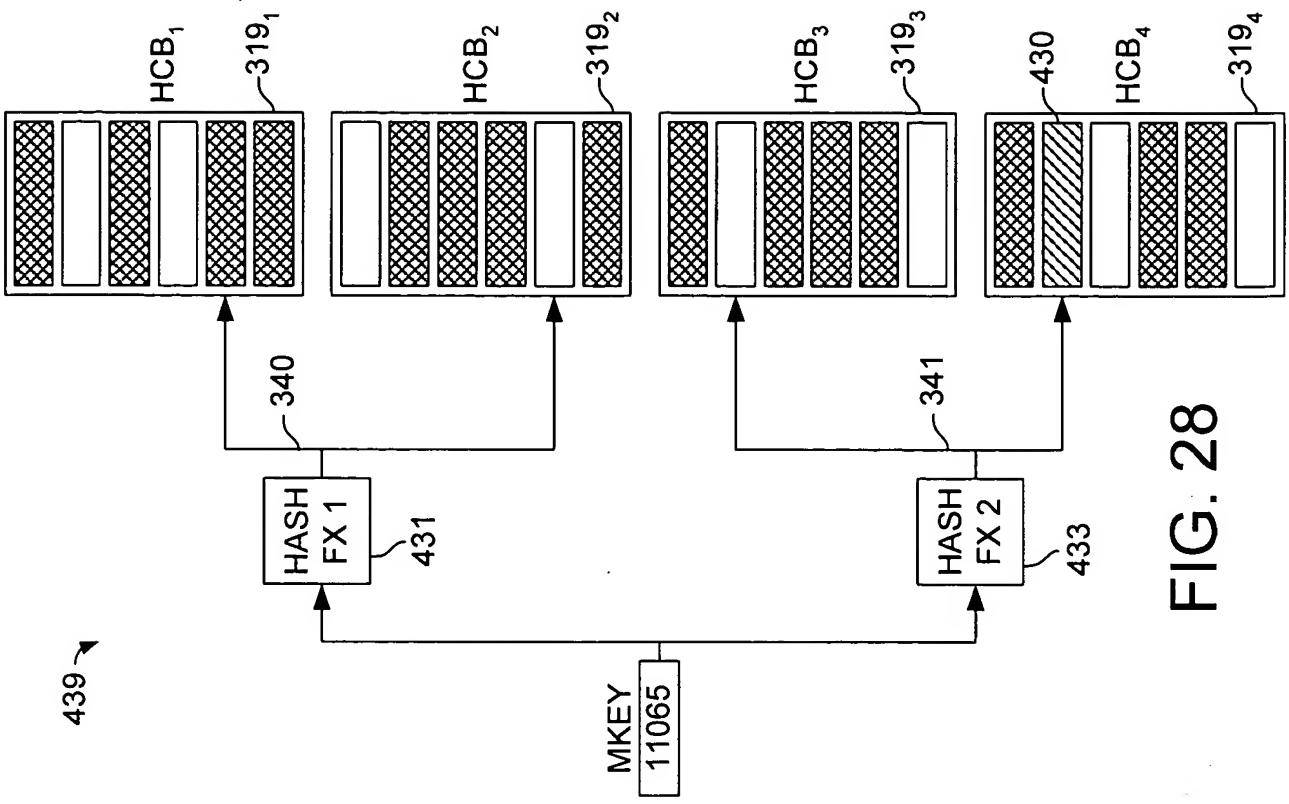


FIG. 28

FIG. 29

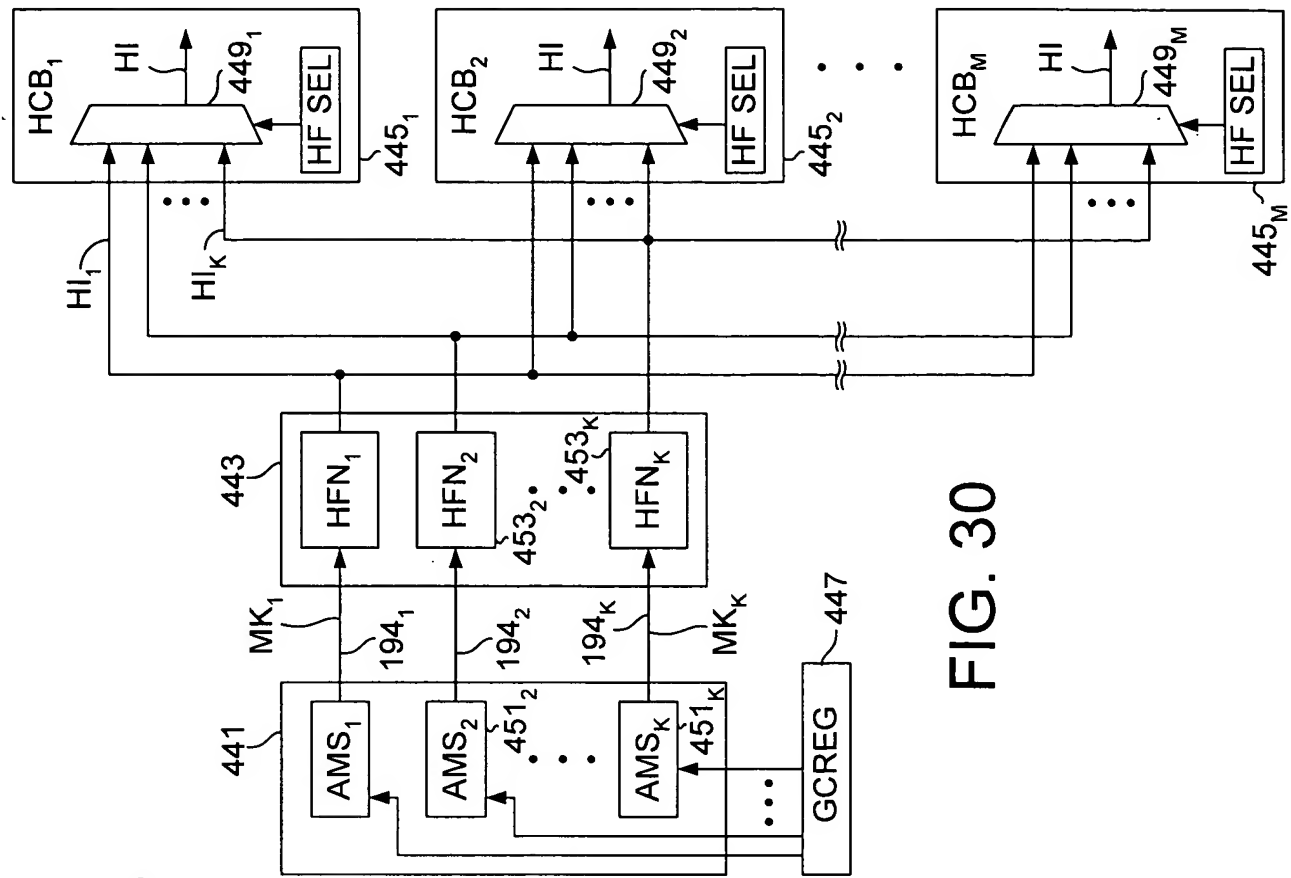
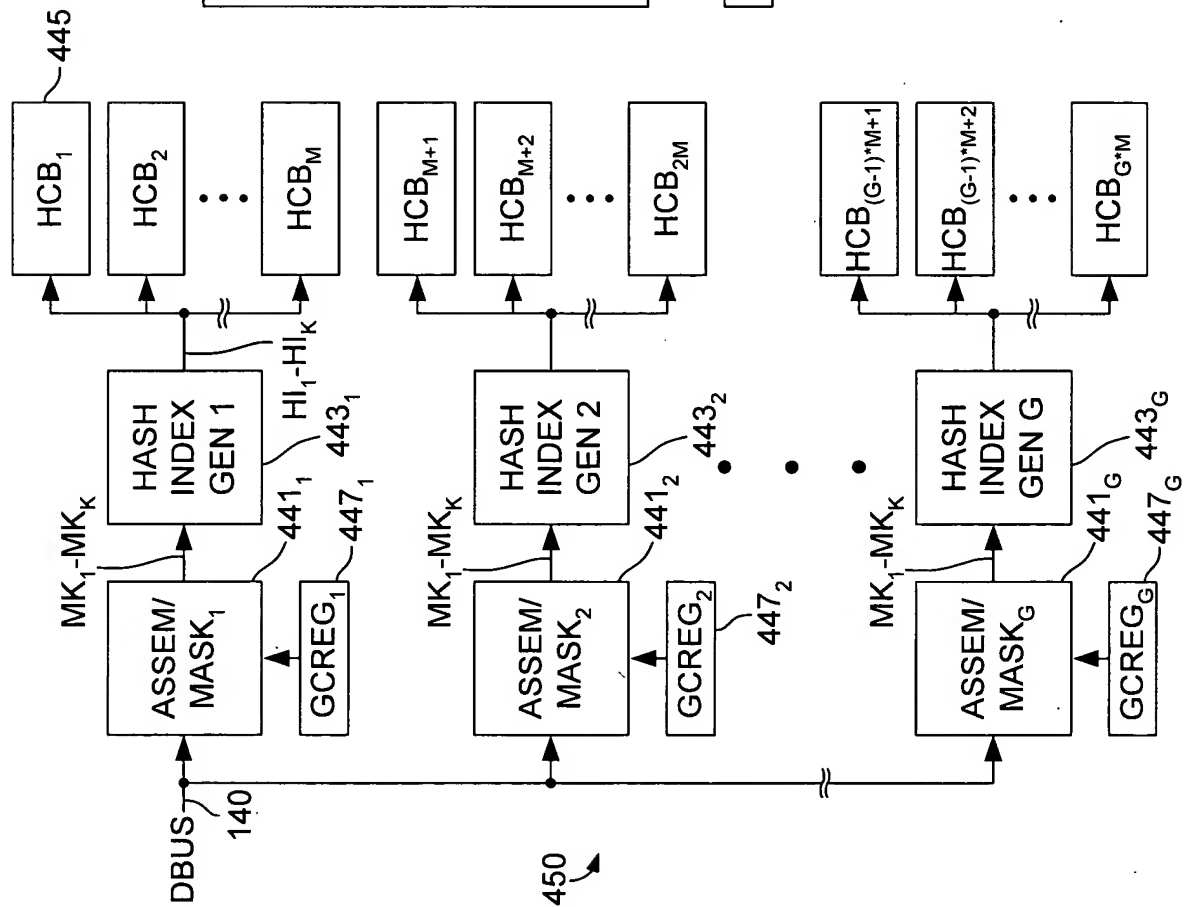


FIG. 30

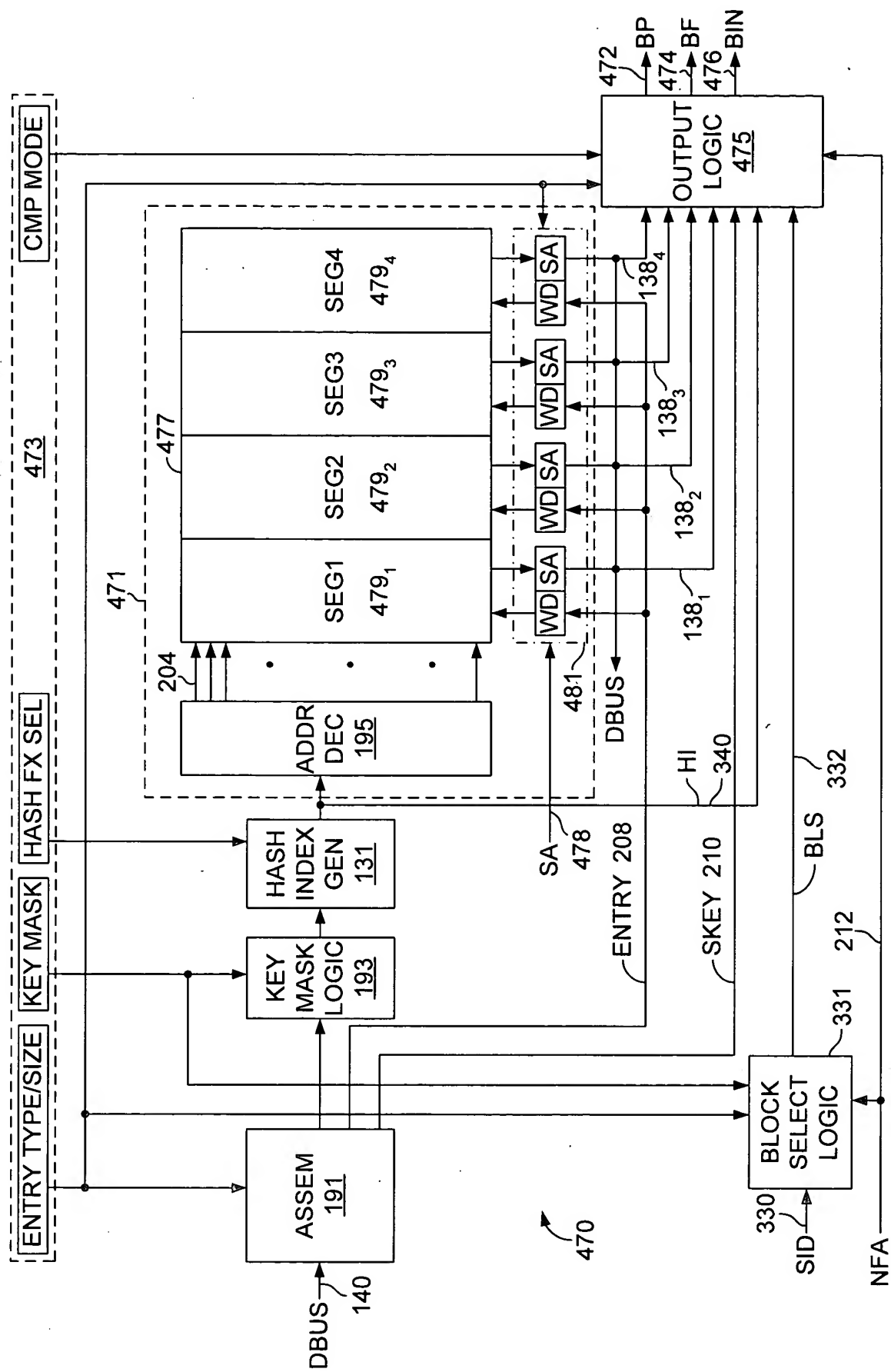


FIG. 31

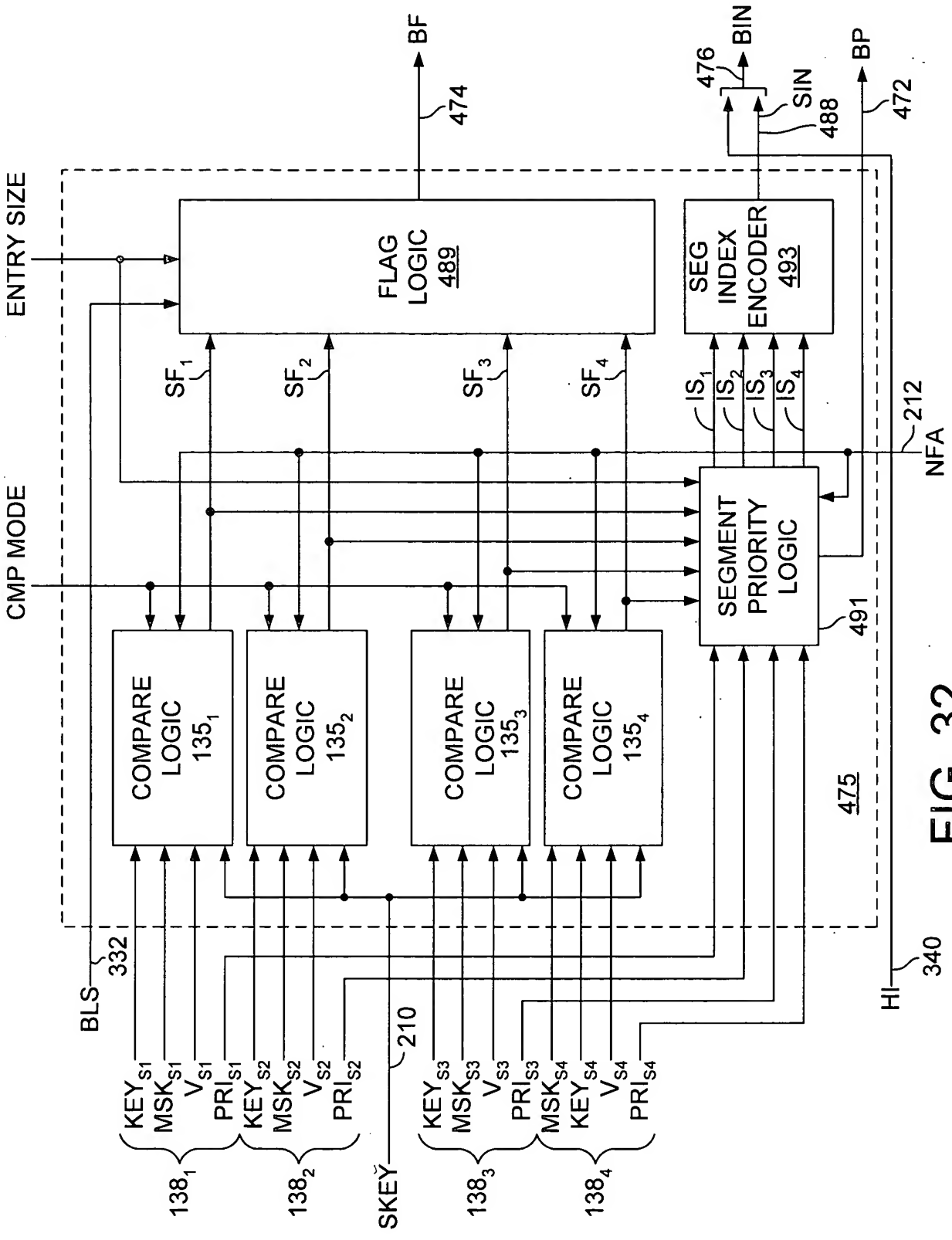


FIG. 32

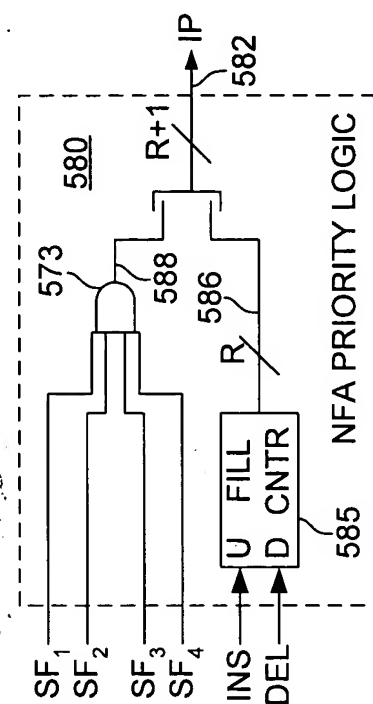


FIG. 33

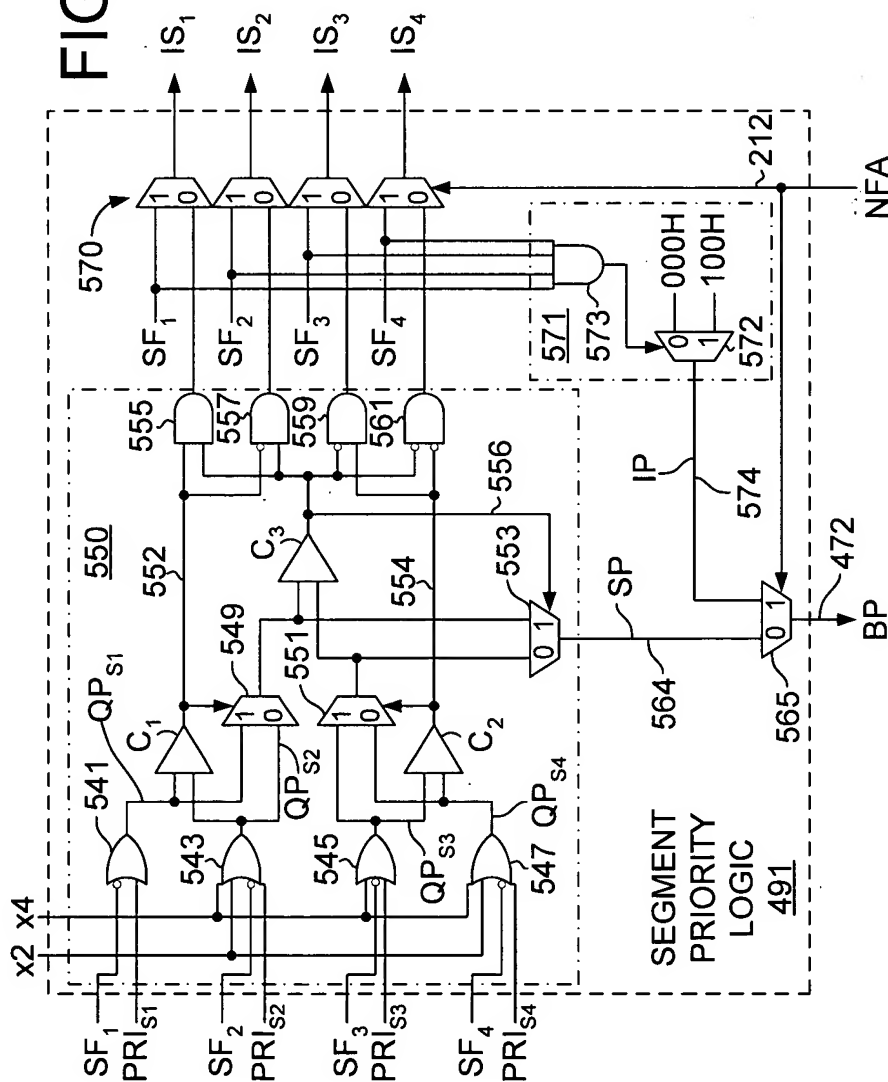


FIG. 34

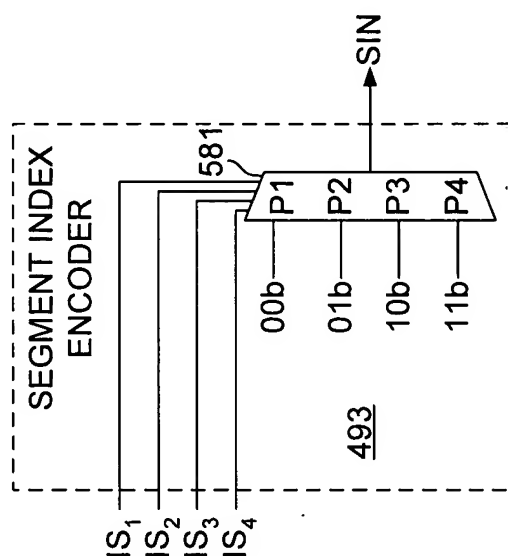


FIG. 36

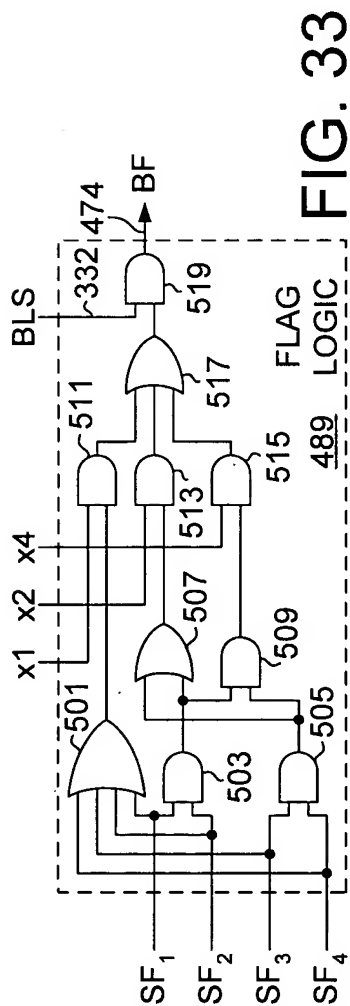


FIG. 35

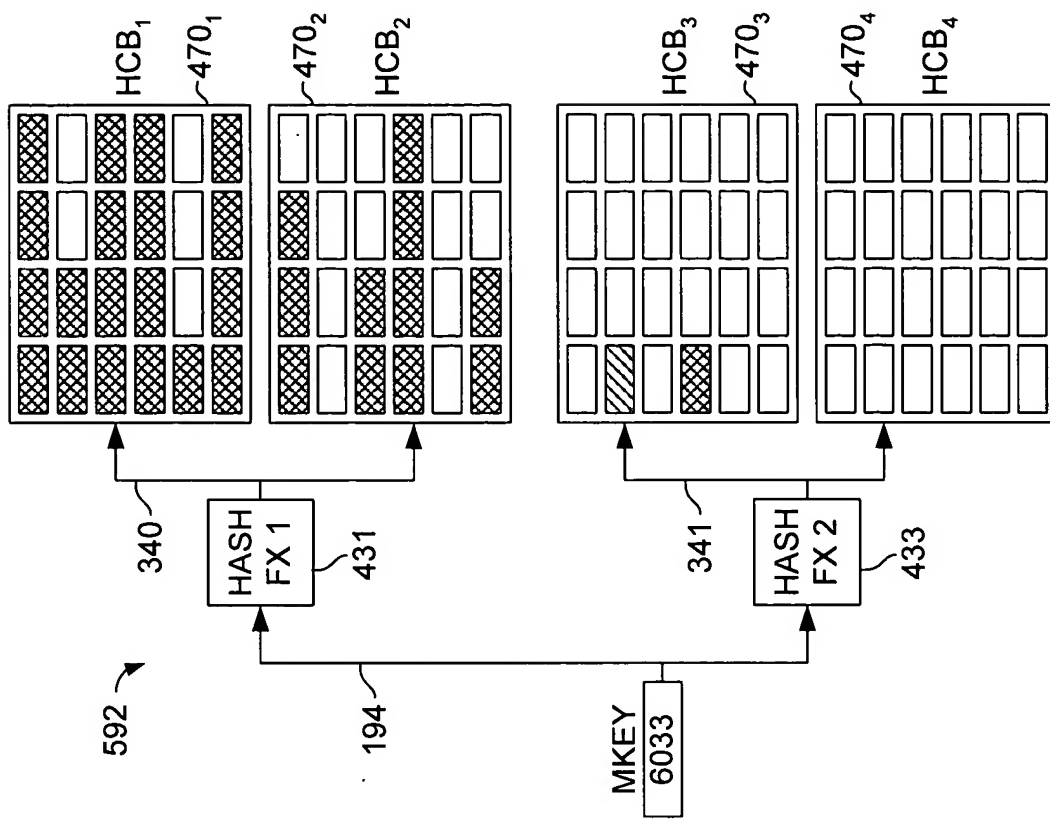


FIG. 37

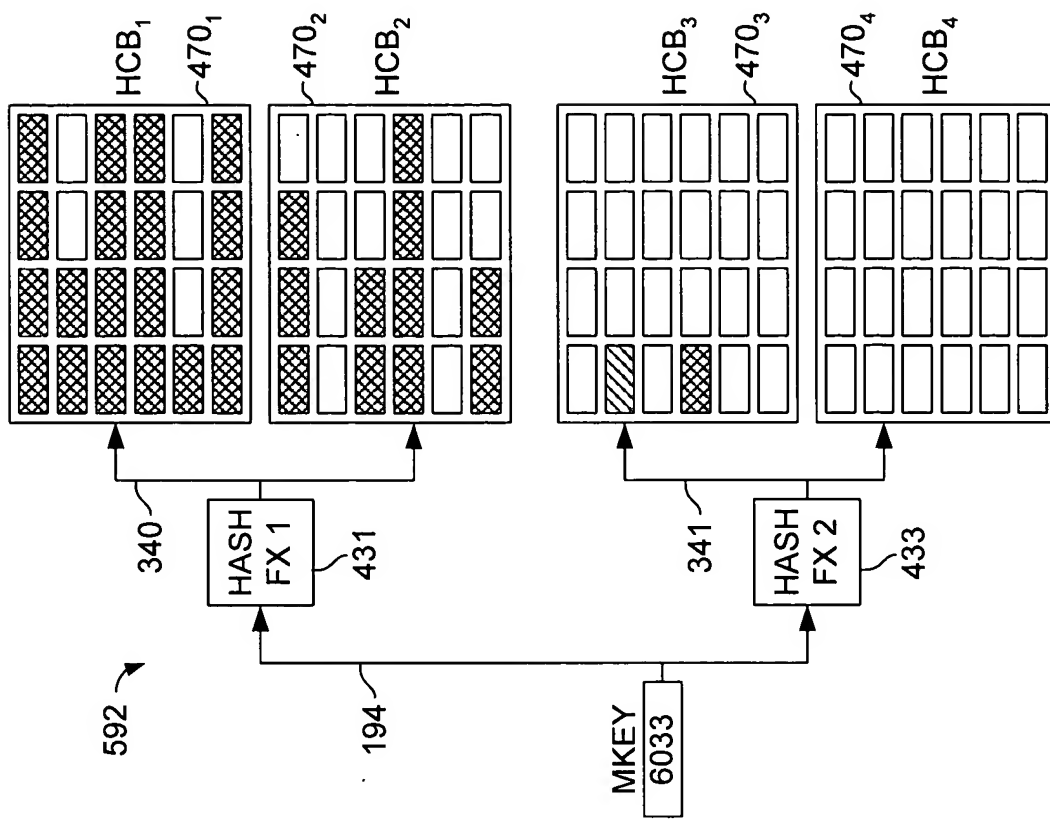


FIG. 38

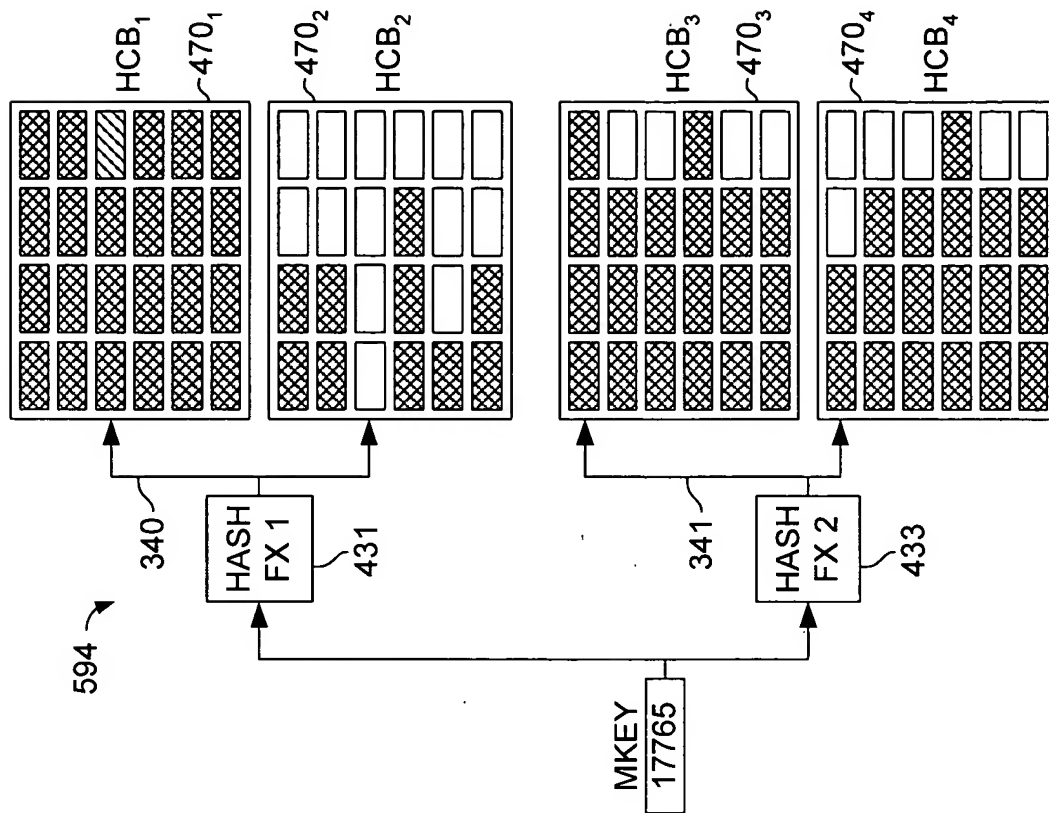


FIG. 39

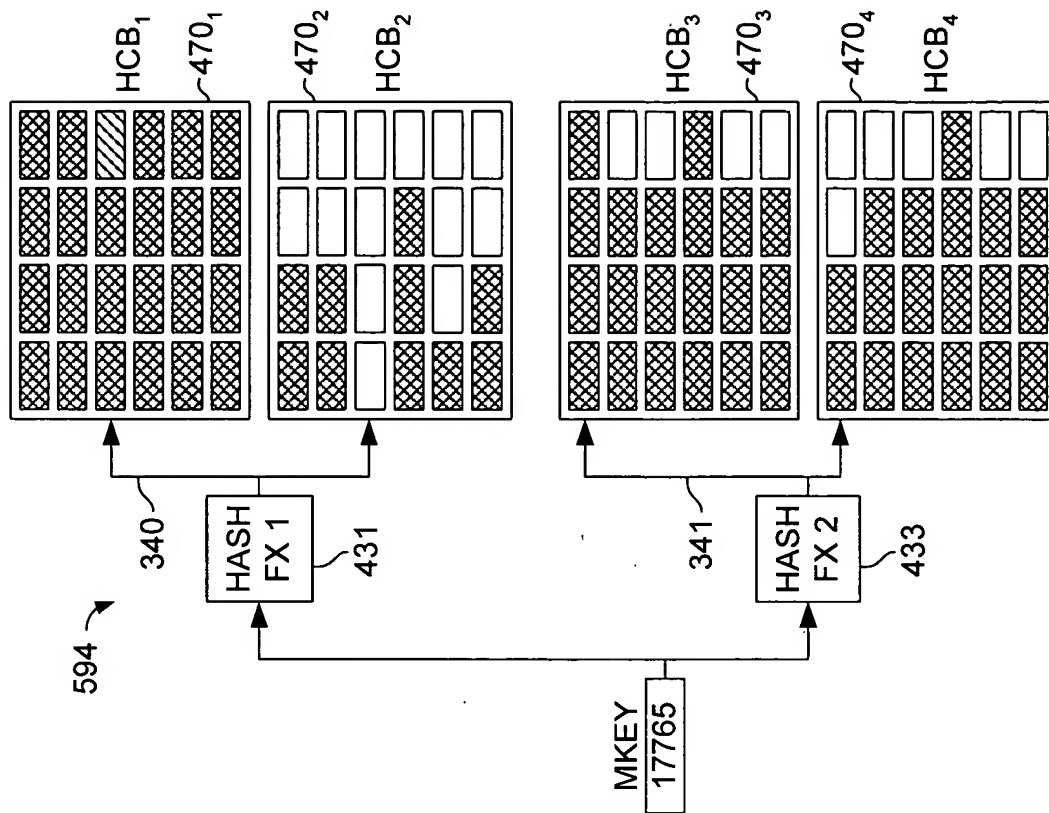


FIG. 40

FIG. 41

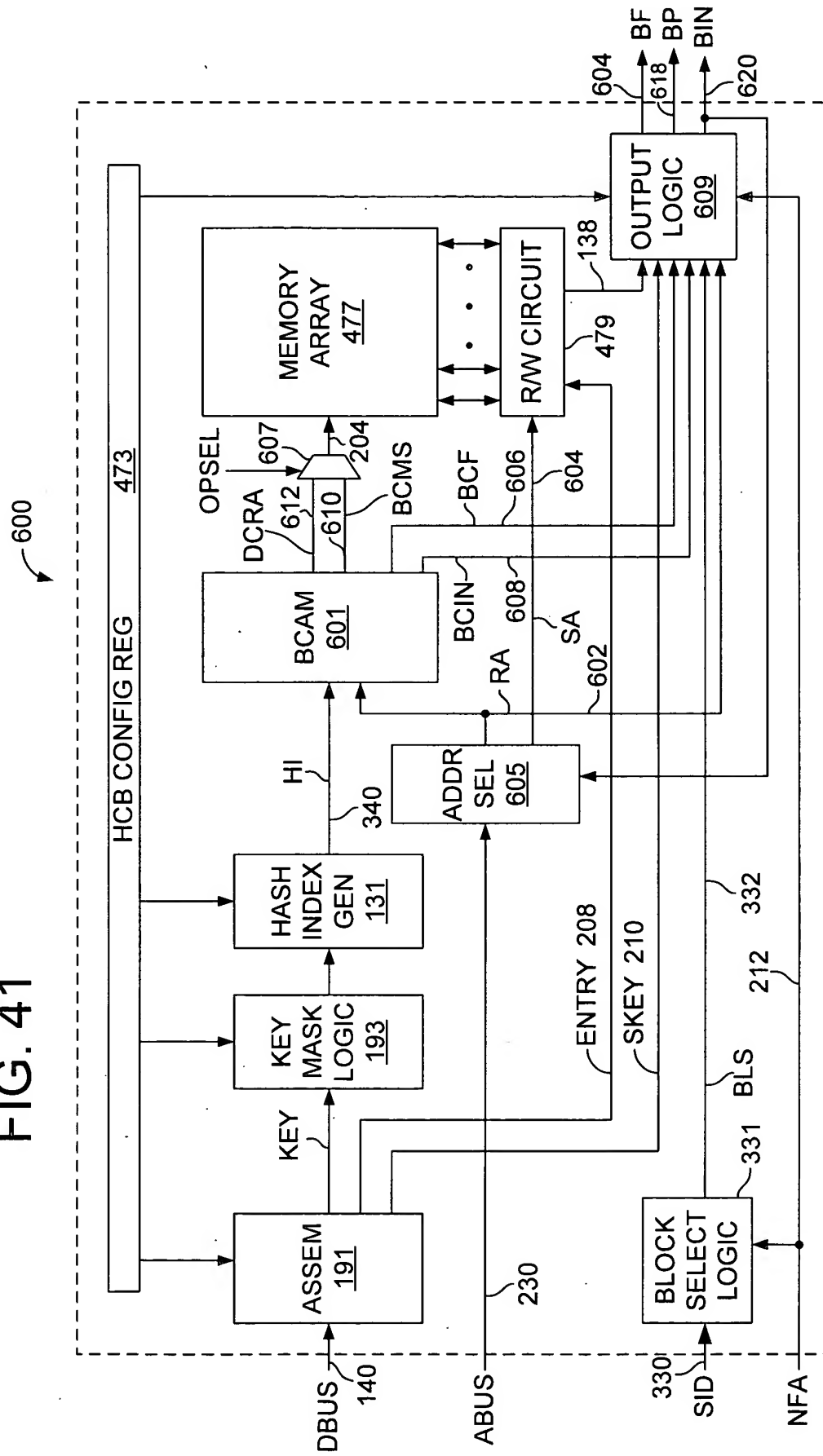
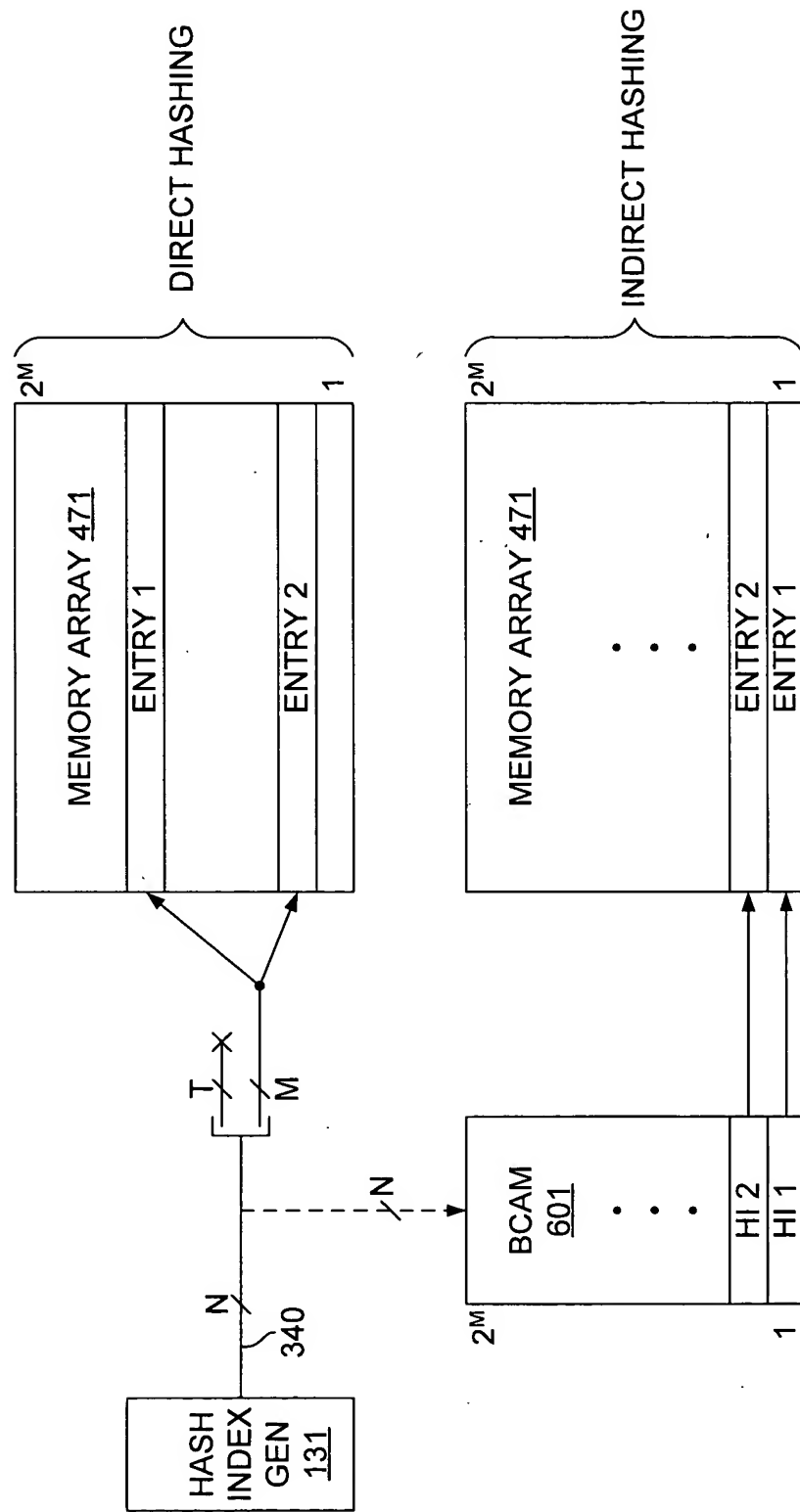
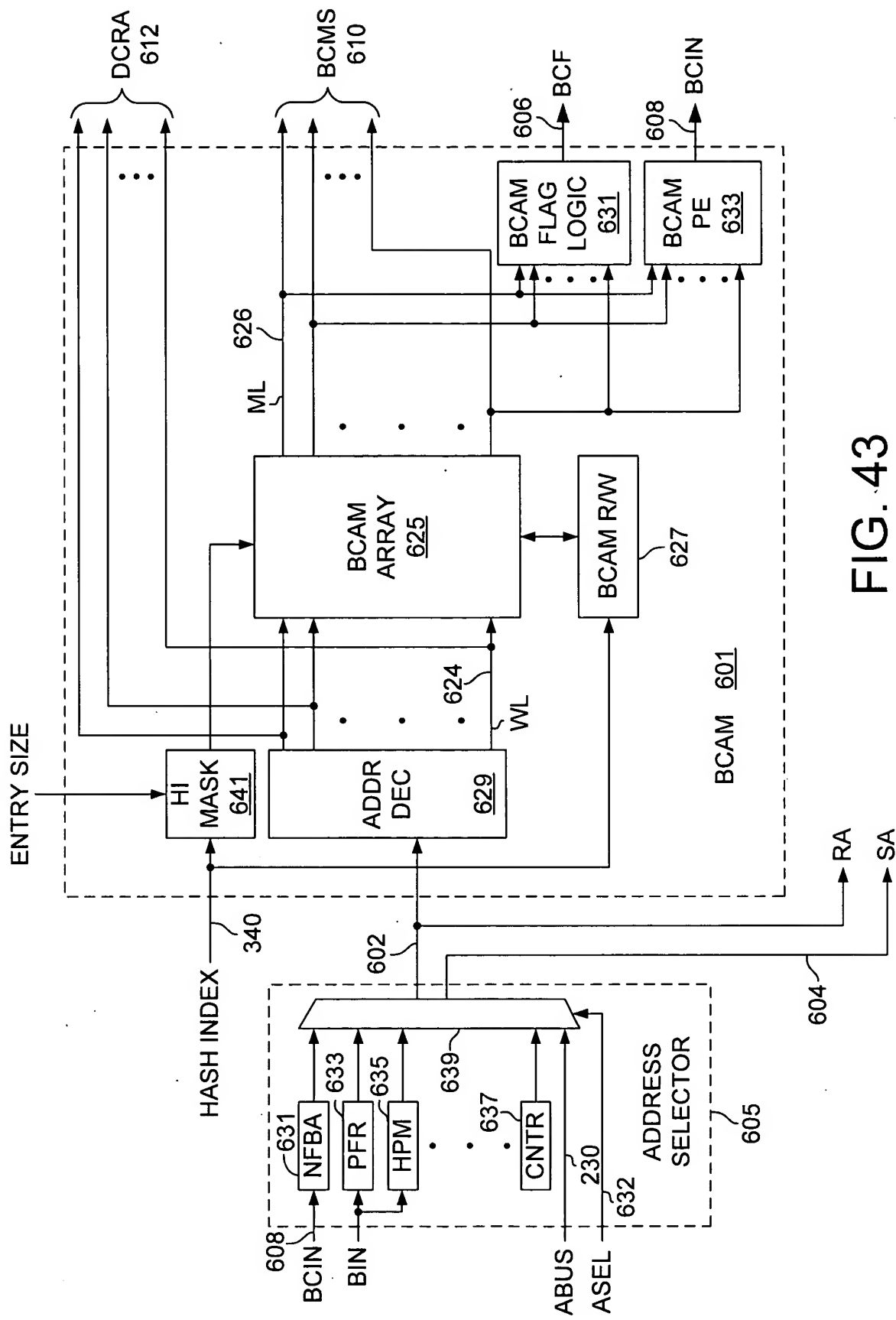
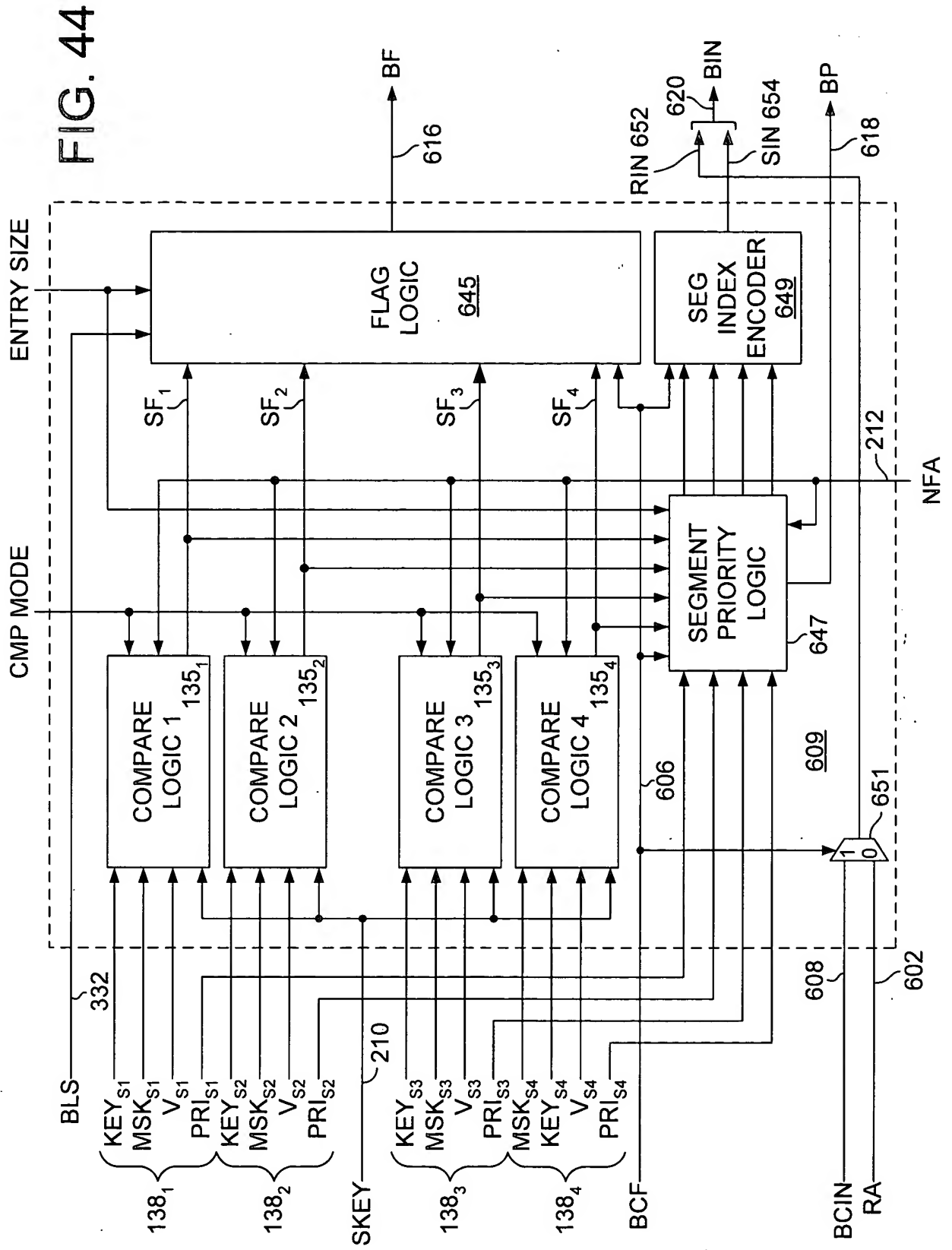


FIG. 42







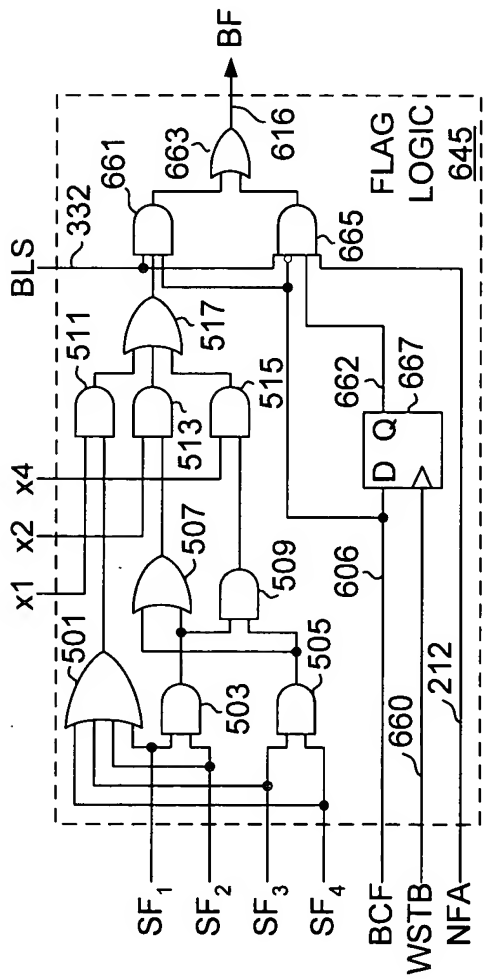


FIG. 45

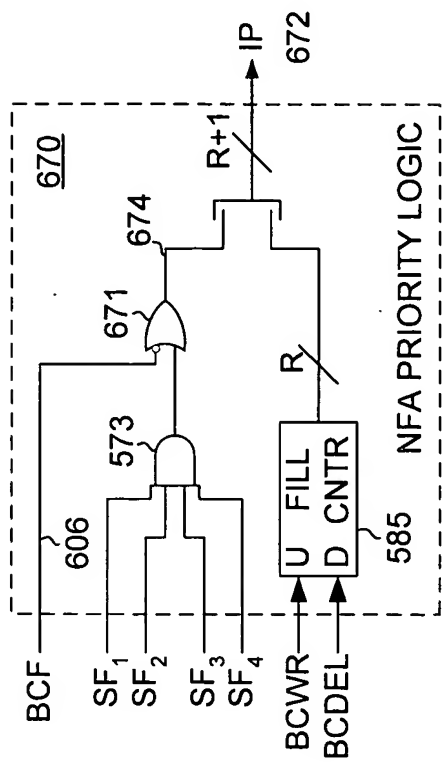


FIG. 46

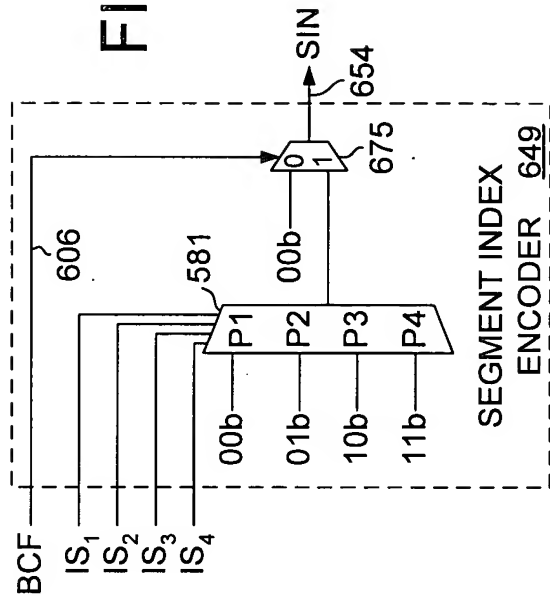


FIG. 47

FIG. 48

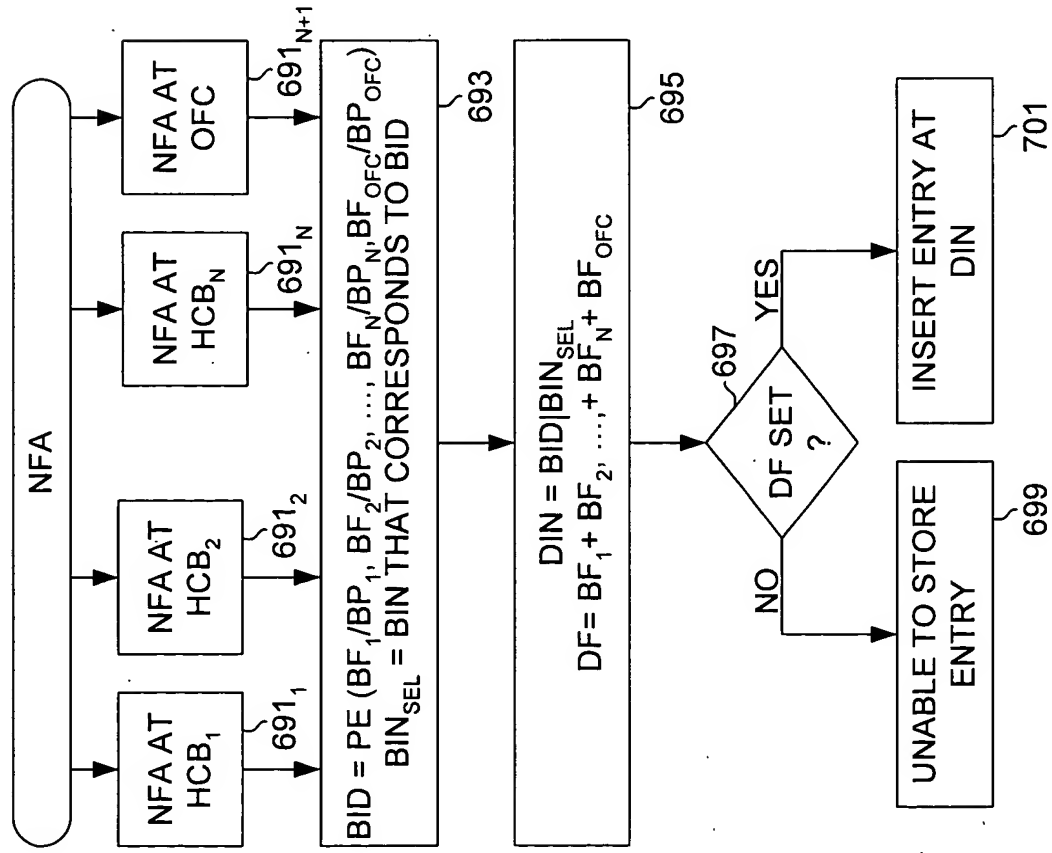


FIG. 49

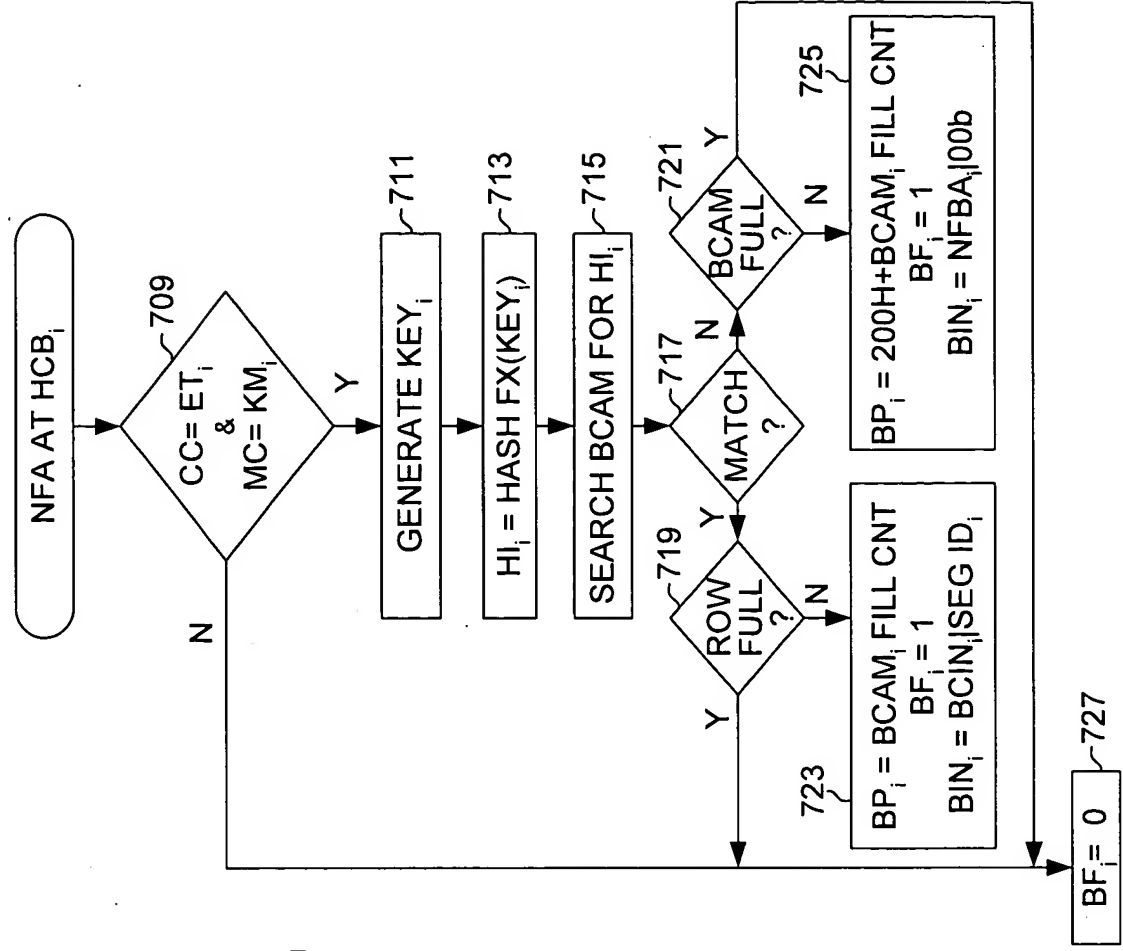


FIG. 50

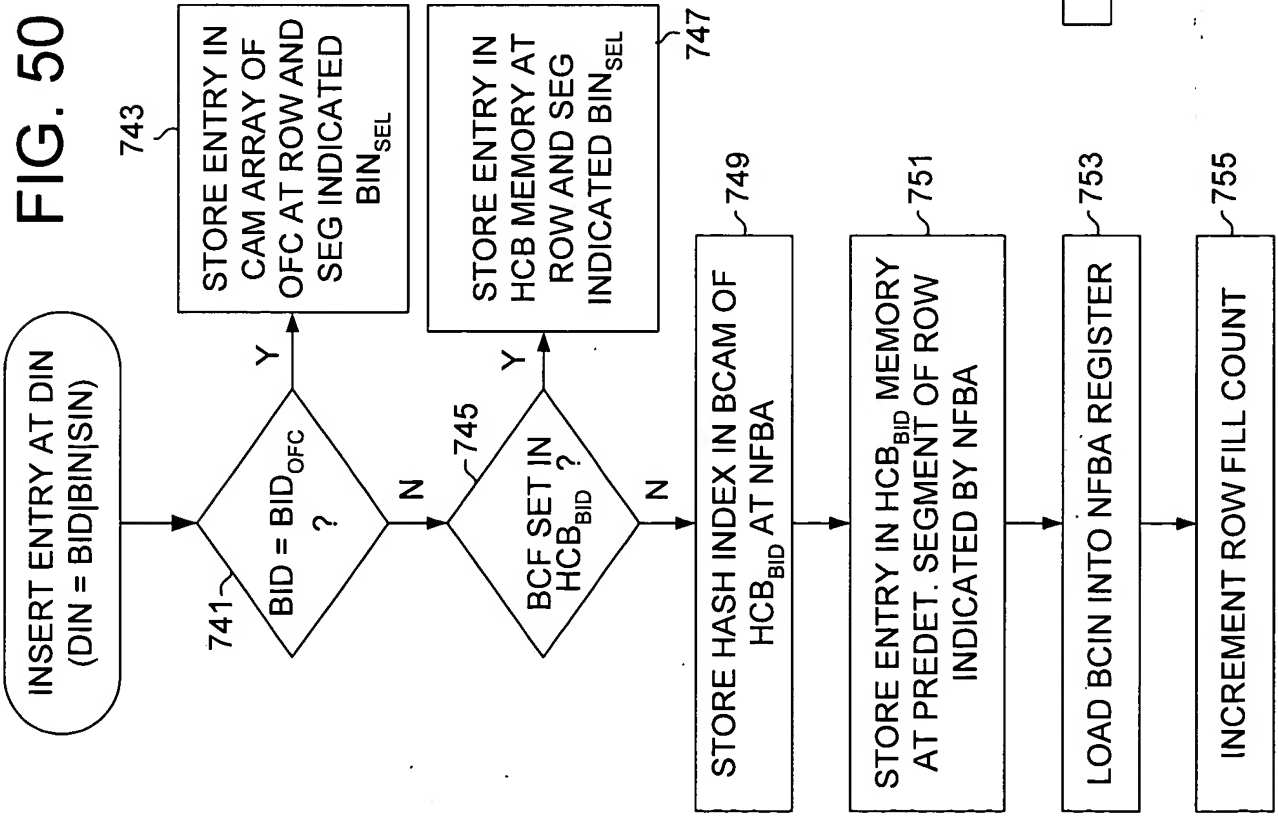
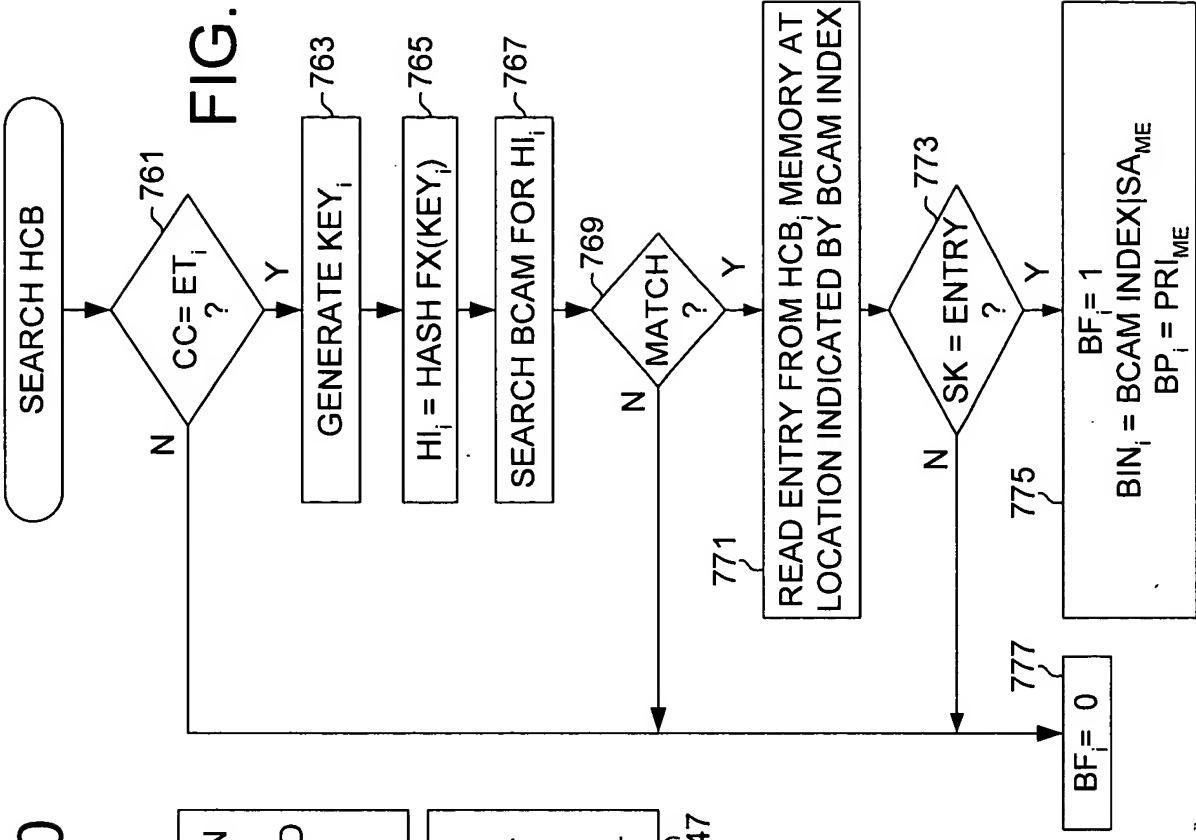


FIG. 51



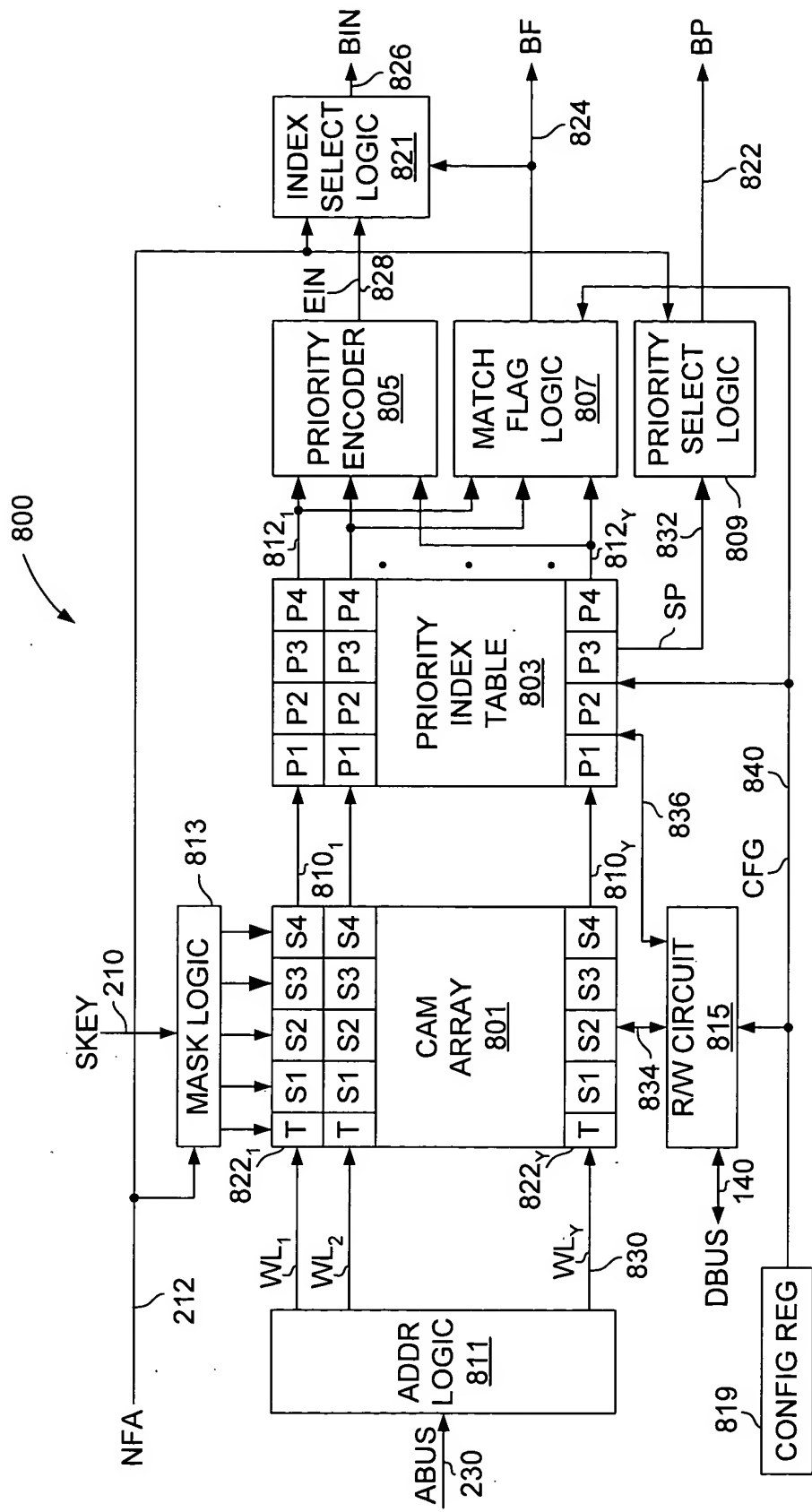


FIG. 52

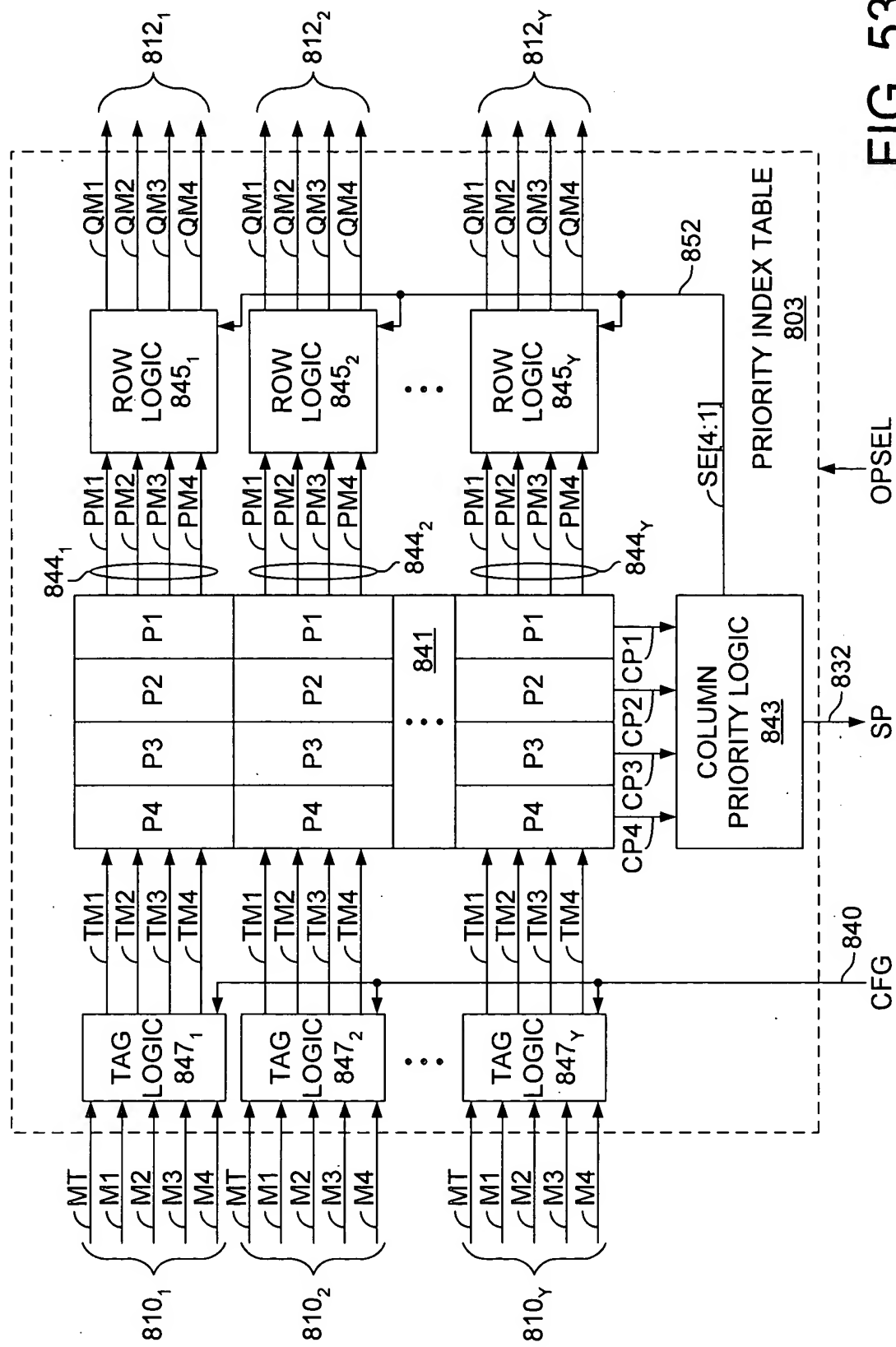


FIG. 53

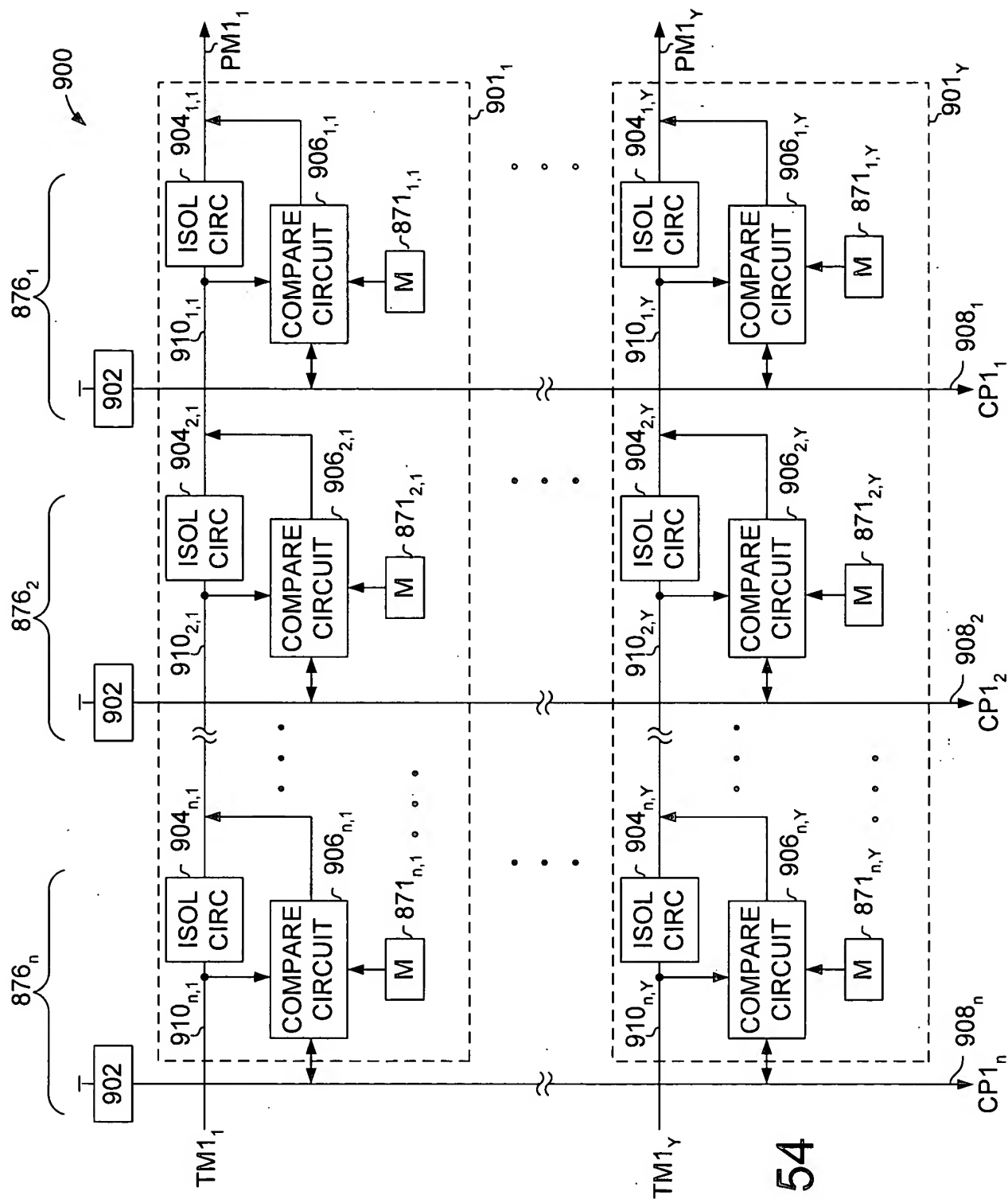


FIG. 54

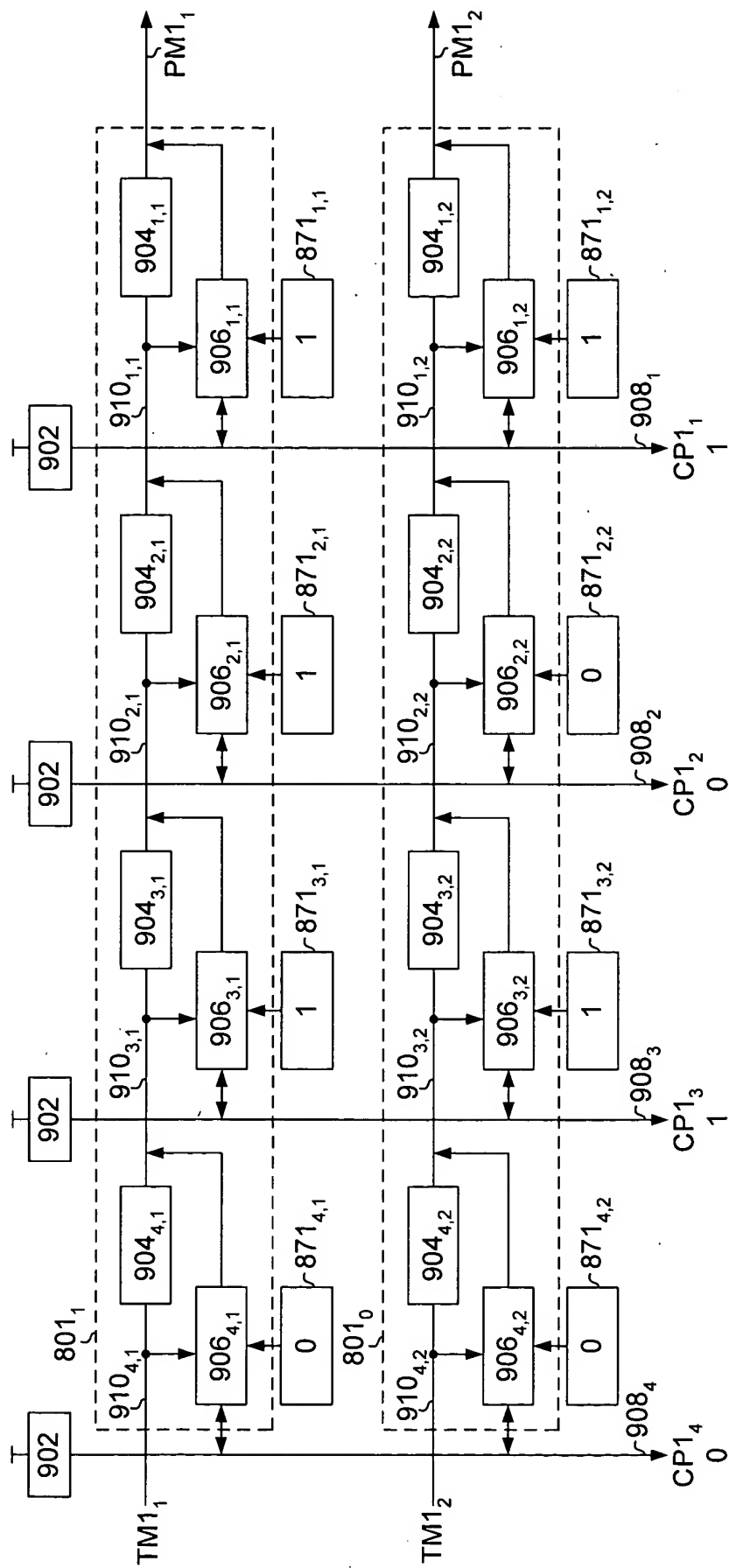


FIG. 55

FIG. 56

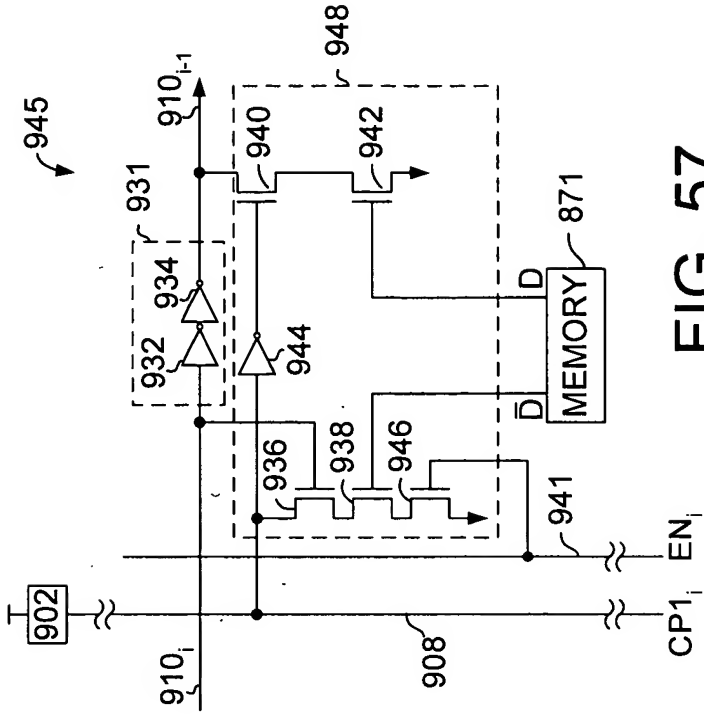
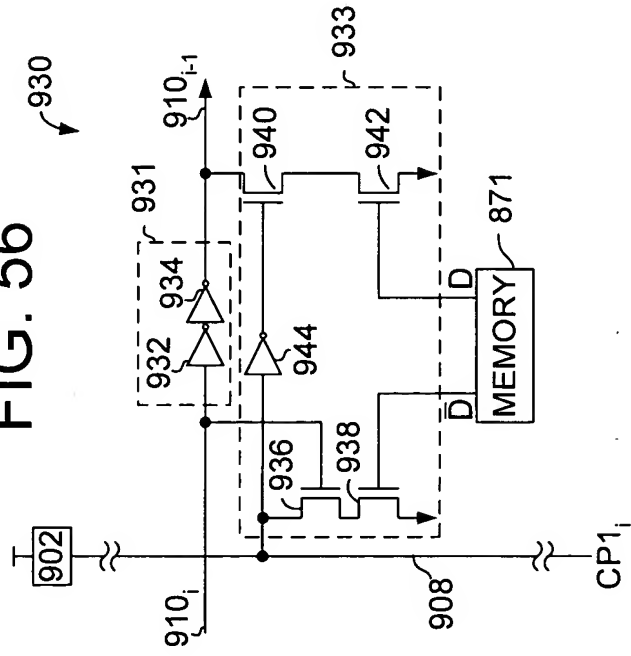


FIG. 57

FIG. 58

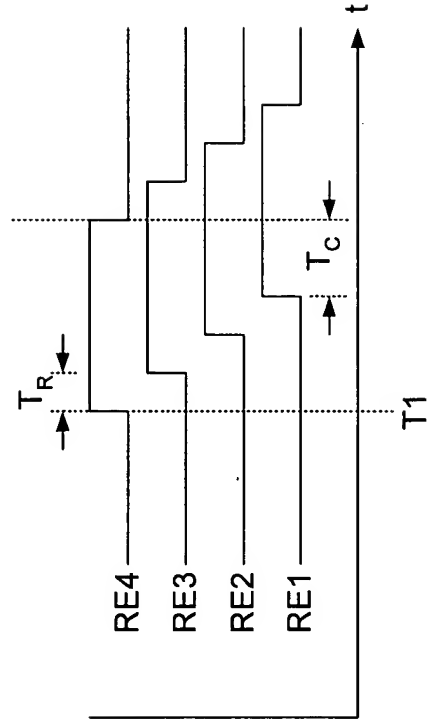


FIG. 59

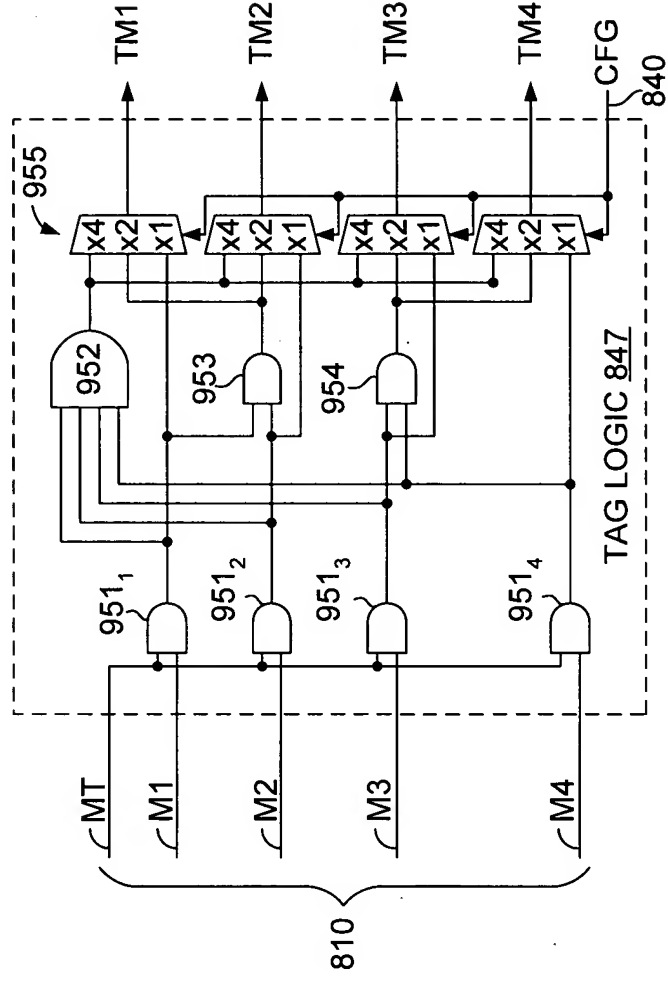
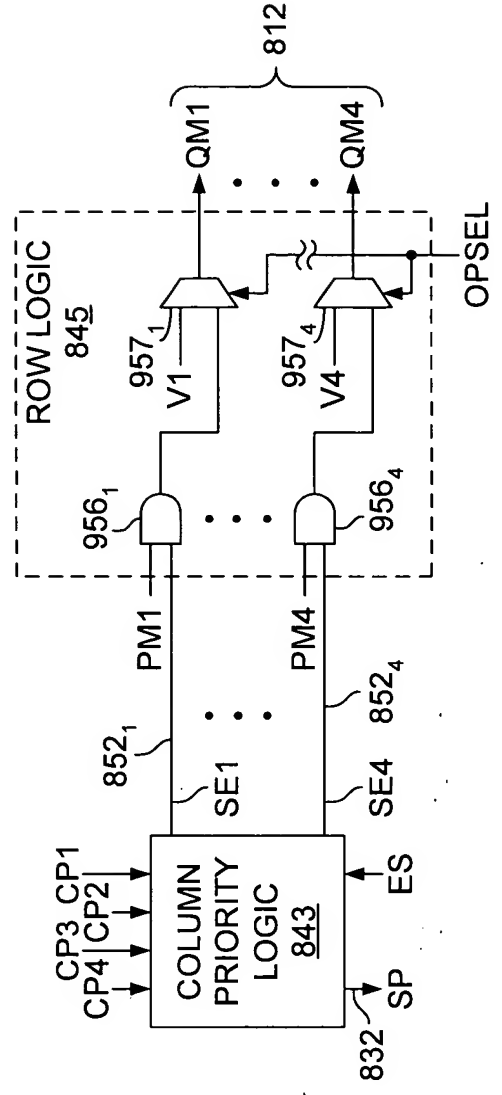


FIG. 60



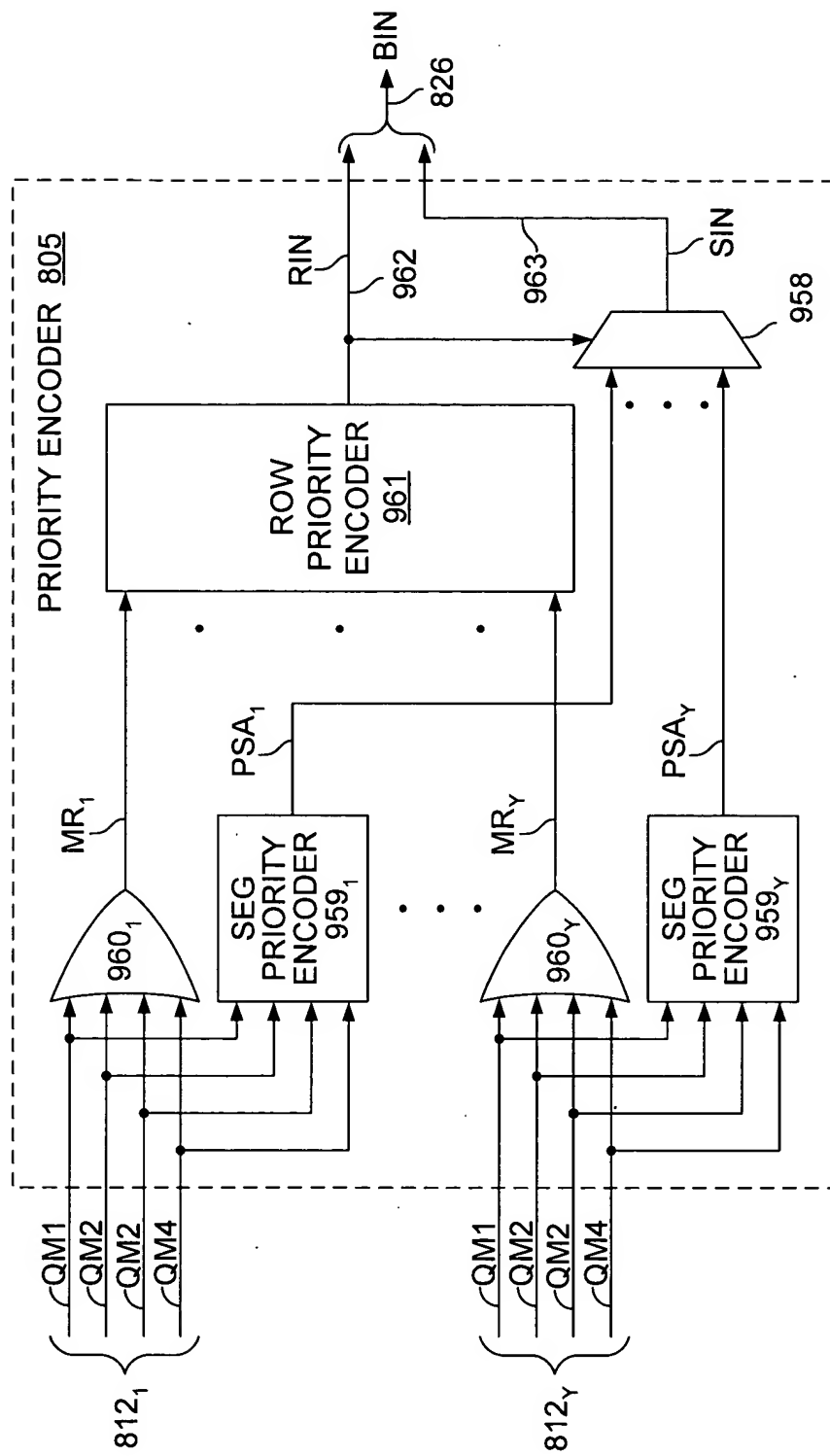


FIG. 61

FIG. 62

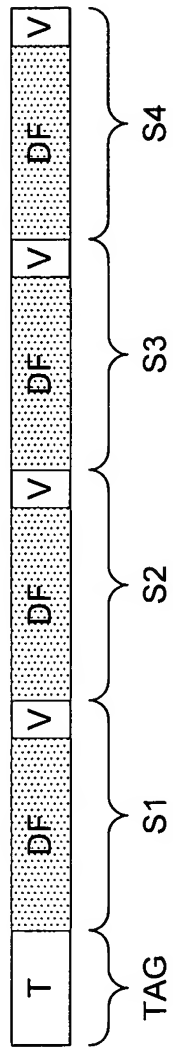


FIG. 63

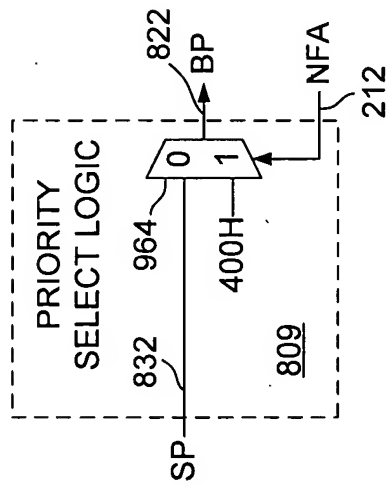


FIG. 64

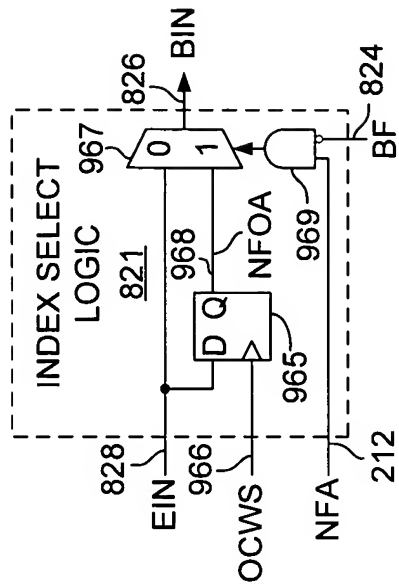


FIG. 65

